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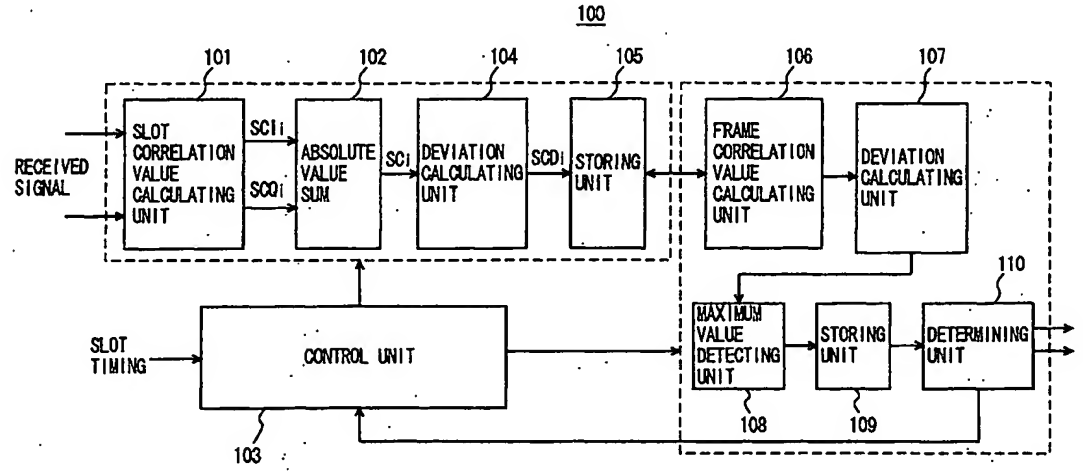
(54) Circuit and method for frame timing detection, cell search apparatus and portable wireless terminal comprising said cell search apparatus

(57) A frame timing detecting circuit, detecting method, cell search apparatus and a portable wireless terminal using such a cell search apparatus are provided. A frame timing detecting unit (100) of a cell search unit (70) of a portable wireless terminal calculates correlation values with all synchronization codes for each slot, deviations thereof are accumulated, and frame correlation values corresponding to scrambling code group numbers are calculated. Maximum values are detected with the slots being shifted, and slot offset number (frame timing) and the corresponding scrambling code group number are detected. Accordingly, the frame timing can be detected with high accuracy regardless of variation in the wireless propagation environment.

FIG. 2



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a frame timing detecting circuit, a frame timing detecting method, a cell search apparatus and a portable wireless terminal using the cell search apparatus. More specifically, the present invention relates to a frame timing detecting circuit and detecting method synchronously capturing a scrambling code for despreading at a receiving side, a cell search apparatus for cell search processing, and a portable wireless terminal including such a cell search apparatus.

Description of the Background Art

[0002] In digital radio communication such as CDMA (Code Division Multiple Access) system, for example, direct sequence spread spectrum communication system has conventionally been employed, in which digital transmission data is scrambled by a spreading code sequence specific to each user and transmitted, and the receiving end descrambles the received digital data by a despreading code sequence.

[0003] At the transmitting end of the digital radio communication using such direct sequence spread spectrum communication system, a spreading unit is provided for generating a spreading code sequence to scramble digital transmission data. At the receiving end, a despreading unit is provided for generating a replica signal of the spreading code sequence to descramble received digital data.

[0004] In the direct sequence spread spectrum communication system, the spreading code used on the transmitting end must be identified on the receiving end, and a start timing of the spreading code on the transmitting end and a start timing of the spreading code on the receiving end must be synchronized with each other.

[0005] Fig. 14 is a schematic block diagram showing a basic structure of a transmitter and a receiver in the direct sequence spread spectrum communication system as discussed above.

[0006] Referring to Fig. 14, the direct sequence spread spectrum communication system is basically constituted of a transmitter 60 of a base station, and a receiver 65 of a mobile station.

[0007] In transmitter 60 of the base station, an original signal to be transmitted is supplied to a primary modulator 61 to narrow the bandwidth of the signal, so as to enable effective use of radiowaves.

[0008] An output of primary modulator 61 is supplied to a spreading unit 62 to be spread, that is, scrambled (secondary modulation) by a spreading code sequence supplied from a spreading code generating unit, not shown, provided therein.

[0009] An output of spreading unit 62 is processed as required for radio communication by a transmission circuit, not shown, and then transmitted via an antenna 63.

[0010] The signal transmitted from antenna 63 is received by an antenna 64 of receiver 65 of the mobile station, processed by a reception circuit, not shown, as required for radio reception, and then supplied to a despreading unit 66.

[0011] Despreading unit 66 despreads, that is, descrambles the received signal by a replica signal synchronized with the spreading code sequence at that receiving end, that is supplied from a spreading code generating unit, not shown, provided therein.

[0012] The original signal is thus derived from despreading unit 66 and demodulated by a demodulating unit 67.

[0013] In order to perform despreading process on receiver 65 of the mobile station in synchronization with transmitter 60 of the base station, it is necessary for despreading unit 66 of receiver 65 of the mobile station to identify the spreading code used at the spreading unit 62 of transmitter 60 of the base station and to capture the start timing thereof.

[0014] In a CDMA communication system, generally, a transmission signal is scrambled in a hierarchical manner using various spreading codes, in the transmitter of the base station side. More specifically, a plurality of symbols spread by a spreading code sequence with a short period together constitute 1 frame of a transmission signal, and by a spreading code sequence having a long period corresponding to 1 frame (hereinafter referred to as a scrambling code), the transmission signal is eventually scrambled with the frame period.

[0015] Therefore, the receiver on the mobile station side (portable wireless terminal) receiving the transmission signal must, at first, descramble the scrambling by the scrambling code. For this purpose, it is necessary to identify the scrambling code used by the base station and to detect the start timing thereof.

[0016] In a conventional CDMA mobile communication system, a base stations synchronous system utilizing GPS (Global Positioning System) has been employed. In the base stations synchronous system, each base station operate referring to time information from one common satellite, and therefore the timing for transmitting each frame of the transmission signal (timing of scramble processing) is perfectly synchronized among base stations. Therefore, what is necessary for each mobile station (portable wireless terminal) is simply to identify the scrambling code used by the base station, and it is unnecessary to detect the start timing of the scrambling code. As identification of the scrambling code is very easy as compared with the detection of the start timing, the base stations synchronous system utilizing GPS advantageously lightens the burden on each mobile station.

[0017] In order to use GPS, however, the base station must be positioned only at such location that can see

through the satellite. Therefore, location of the base station is limited.

[0018] Standardization of wide-band CDMA (Wide-Band Code Division Multiple Access) system, which is a mobile communication system of the next generation, has been standardized by a project named 3rd Generation Partnership Project (3GPP). According to the wide band CDMA system specification, not the base stations synchronous system utilizing the GPS described above but a base stations asynchronous system not using the GPS is determined to be adopted. Details of such a mobile communication system of the next generation is described in 3GTS25.213v3.3.0, which is a specification of 3GPP.

[0019] In the base stations asynchronous system, different from the base stations synchronous system described above, each base station operates at an arbitrary timing independent from each other, and transmits each frame of the transmission signal after scramble processing. Thus, it is necessary for each mobile station to identify the scrambling code used by the base station and, in addition, to detect the start timing of the scrambling code.

[0020] More specifically, though the frame formats of the transmission signals from base stations are common among base stations, the timings of the head positions are not aligned. Therefore, it is necessary to detect a boundary (start timing) of the transmission signal frame in order to descramble.

[0021] More specifically, it is necessary for each mobile station to detect the start timing of the scrambling code and thereafter to specify the scrambling code. Such a series of operations is generally referred to as "cell search".

[0022] Cell search is necessary, for example, in the following situation.

[0023] First, immediately after the mobile station (portable wireless terminal) is powered on (initial synchronization), it is necessary to detect the start timing of the frame and to identify the scrambling code.

[0024] Further, when base station as a connection destination changes (a so-called hand over) as the mobile station moves, the base station which is communicating notifies mobile station of the information of the base station as a hand over destination (including scrambling code information) in advance, and therefore, it is necessary for the mobile station to detect the start timing of the frame, though it is unnecessary to identify the scrambling code.

[0025] Cell search for the mobile station of the base stations asynchronous system requires a very complicated processing to detect the start timing of the transmission signal frame (scrambling code) from a base station, and hence it takes a long time for the detection process.

[0026] Fig. 15 is a functional block diagram representing a configuration of a cell search unit 70 performing the above described cell search process, in a mobile station of the base stations asynchronous system. Cell search unit 70 is included in despreading unit 66 of receiver 65 of the mobile station shown in Fig. 14, and it first receives the signal transmitted from the base station and generates information specifying the timing and the type of the scrambling code necessary for descrambling (despreading process).

[0027] The cell search is generally executed in a process including three steps, as shown in Fig. 15. Specifically, cell search unit 70 includes a slot timing detecting unit 71, a frame timing detecting unit 72, a scrambling code detecting unit 73 and a control unit 74.

[0028] More specifically, when it is necessary to detect the timing and to identify the type of the scrambling code at the time of initial synchronization as described above, the processing of the first stage detecting the slot timing is performed by slot timing detecting unit 71, the process of the second stage detecting the scrambling code group number and frame timing is performed by the frame timing detecting unit 72, and the process of the third stage identifying the scrambling code is performed by the scrambling code detecting unit 73.

[0029] The operation which will be described later by the configuration represented by the functional block diagram of Fig. 15 is executed in a hardware manner, or in a software manner using a digital signal processor (DSP).

[0030] In the following example, it is assumed that, in accordance with 3GPP specification, 1 frame of the transmission signal from a base station includes 15 slots, there are 512 different types of scrambling codes used for scrambling on the base station, the 512 different scrambling codes are classified into 64 scrambling code groups (each corresponding to 8 types of scrambling codes), and a synchronizing channel is arranged at every head symbol position of all the slots (each slot being formed of a plurality of symbols) constituting the frame.

[0031] First, the process of the first stage performed by slot timing detecting unit 71 will be described. The transmission signal from a base station includes a control channel signal and an information channel signal. Fig. 16 is a schematic diagram representing a control channel signal format in accordance with the aforementioned 3GPP standard. The process of the first stage is to detect the timing of the boundary of every slot constituting a frame.

[0032] The control channel is further divided into a P-SCH (Primary Synchronization Channel) and S-SCH (Secondary Synchronization Channel). The former is referred to as a first synchronization channel and the latter is referred to as a second synchronization channel.

[0033] Here, P-SCH and S-SCH are control channels spread by spreading code sequences of 256 chips of different types (first synchronization code and second synchronization code) which are orthogonal with each other, and multiplexed with equal level (without any weight) at the head symbol position (#0) of every slot

constituting the frame, as shown in Fig. 16.

[0034] More specifically, each of P-SCH and S-SCH represents a channel spread by a spreading code sequence of 256 chips formed of a code sequence of 1 and 0. At the head symbol position of each slot, the two code sequences are supplied in parallel without any weight (with same transmitting power) on the transmitting side, and a result of addition of corresponding chip positions with each other regarding 1 as -1 and 0 as +1 is transmitted at the head symbol position, as a synchronous channel signal. In other words, on the control channel signal format shown in Fig. 16, the signal is actually carried only at the head symbol position of each slot.

[0035] The head symbol position of each slot at which the synchronization channels are multiplexed is masked at the time of scrambling on the base station side, and except for the head symbol position of each slot, scrambling with a prescribed scrambling code is performed on the entire frame.

[0036] In despreading unit 66 (Fig. 14) of the receiver of the mobile station, the reception signal of the control channel is divided into I phase (in-phase component) and Q phase (quadrature component), and commonly applied to a correlation processing unit 71a of slot timing detecting unit 71, a correlation processing unit 72a of frame timing detecting unit 72 and a correlation processing unit 73a of scrambling code detecting unit 73.

[0037] In the first stage of the cell search process, slot timing detecting unit 71 detects P-SCH multiplexed at the head symbol position of each slot, so as to detect the start timing of every slot constituting the frame.

[0038] This is possible as the control channel P-SCH at the head symbol position of each slot is spread by a known spreading code (first synchronization code) of 256 chips common to all the base stations.

[0039] The I phase component and the Q phase component of the received control channel signal are correlated with the aforementioned known first synchronization code supplied from a first synchronization code generating unit 71b, respectively.

[0040] More specifically, correlation processing unit 71a includes a first digital matched filter, not shown, for calculating a correlation value between the I phase component of the received control channel signal and the first synchronization code, and a second digital matched filter, not shown, for calculating a correlation value between the Q phase component of the received control channel signal and the first synchronization code.

[0041] The digital matched filter detects, by a product-sum operation of a received signal and the spreading code, correlation value peak of these two. The digital matched filter is described in detail, for example, in Tajika, Journal of the Institute of Electronics, Information and Communication Engineers, SST62-21, "Digital Matched Filter Technique in Spread Spectrum Communication and Problems Thereof". Therefore, detailed description thereof will not be given here.

[0042] In correlation processing unit 71a, correlation value outputs of first and second digital matched filters, not shown, are power-added by an adder, not shown, and applied to a path search unit 7c.

[0043] Correlation processing unit 71a calculates the correlation value with known first synchronization code, for every slot constituting the frame, in the manner as described above. As the P-SCH spread by the first synchronization code of 256 chips is multiplexed only at the head symbol position of each slot as described above, it is the case that when the correlation value between the signal in the slot and the first synchronization code is found by the digital matched filter for each slot, a correlation value peak is obtained at the head position of the slot (though P-SCH spread by the second synchronization code is also multiplexed, the first and second synchronization codes are orthogonal with each other, and therefore, it is possible to separate and detect the correlation value peaks from each other by the digital matched filter).

[0044] The correlation value output of 1 slot obtained in this manner is stored in a memory, not shown, of the path search unit 71c.

[0045] The correlation value output is calculated in the similar manner for the next slot, and accumulated to the correlation value output of the immediately preceding slot that has been calculated and held in the memory. When such accumulation is performed for a plurality of slots, noise component is reduced by averaging process, and hence a correlation value peak position in one slot section can be detected.

[0046] The timing of the detected correlation value peak is detected as a timing of the head symbol position of the slot, that is, the slot timing, and the detected slot timing is applied to control unit 74.

[0047] The second stage process by the frame timing detecting unit 72 will be described next. The second stage process is to detect a timing of the boundary of each frame, and to detect to which of the 64 scrambling code groups the scrambling code used for scrambling the frame on the base station belongs.

[0048] In the second stage of cell search, frame timing detecting unit 72 monitors the S-SCH multiplexed at the head symbol position of each slot, to detect the frame timing and to specify the scrambling code group.

[0049] This is because the control channel S-SCH at the head symbol position of each slot is spread by one of 16 different second synchronization codes (SSC0-15) of 256 chips, different from the first synchronization code described above.

[0050] As described above, according to the 3GPP standard, there are 512 scrambling codes used for scrambling, which are classified into 64 groups, each including 8 types. Corresponding to each of 64 groups, combinations of second synchronization codes are defined, in which one of 16 different second synchronization codes is allocated to respective ones of 15 slots #1 to #15 constituting 1 frame. The table of Fig. 17 shows correspondence between the scrambling code group

numbers 1-64 (ordinate) and any of 16 types of second synchronization code numbers that are allocated corresponding to the slot numbers #1 to #15 (abscissa) of 1 frame for every scrambling code group number.

[0051] More specifically, it is the case that S-SCH multiplexed at the head symbol position of respective slots #1 to #15 of 1 frame of the control channel signal transmitted from the base station is spread in accordance with the combination of the second synchronization codes corresponding to any of the scrambling code group numbers 1 to 64 shown in the table of Fig. 17.

[0052] Therefore, when it is possible to specify what combination of the second synchronization codes was used for spreading 15 slots constituting a certain frame, it is possible to specify the scrambling code group number corresponding to the combination.

[0053] In the second stage, for each of the 15 slots constituting 1 frame, correlation values with all of the 16 different types of second synchronization codes are calculated, and the results are temporarily stored. Thereafter, 64 different accumulated values of the correlation values corresponding to the combinations of the second synchronization codes for respective ones of the group numbers 1 to 64 are calculated, and that scrambling code group number which corresponds to the combination of the second synchronization codes having the largest accumulated value of the correlation values is specified from numbers 1 to 64.

[0054] Such process of the second stage will be more specifically described in the following.

[0055] First, correlation processing unit 72a of frame timing detecting unit 72 receives from control unit 74 a signal indicative of the timing of the head symbol position of each slot detected in the first stage process described above, calculates 16 different correlation values between the head symbol and all of 16 different second synchronization codes (SSC0 to 15) for each slot, and stores the calculated values in a memory, not shown, of scrambling code group detecting unit 72c.

[0056] This process is performed for each of 15 slots constituting 1 frame. All the correlation values stored in the memory as a result will be represented as C (i, j) (i= 0, 1, ..., 14, j = 0, 1, ..., 15). Here, i is a number specifying 15 slots, and j is a number specifying 16 different second synchronization data. Therefore, in the memory, there are the correlation values C (0, 0) to C (14, 15) stored therein.

[0057] Thereafter, scrambling code group detecting unit 72c calculates, in accordance with the table of combinations of the second synchronization codes shown in Fig. 17, the accumulated value of the stored correlation values of all the slots of numbers #1 to #15 calculated with the second synchronization codes of the corresponding combination, for each scrambling code group number. As it is not always the case that 15 slots as the object of accumulation start from the head of the frame (boundary) (the number of slots shifted from the boundary will be referred to as a slot offset), the slots are shifted one slot by one slot for each scrambling code group number while calculating accumulated values of correlation values of 15 slots with every shift of the slots. In this manner, for each scrambling code group number, the slots are shifted up to 14 slots while at every shift repeating accumulation of correlation values of 15 slots, whereby 15 different correlation value accumulated values (power addition values) are obtained finally.

[0058] This process is performed for every one of 64 scrambling code groups. All the power addition values stored in the memory as a result will be represented as P (I, m) (I = 0, 1, ..., 63, m = 0, 1, ..., 14). Here, I represents a number specifying 64 scrambling code groups, and m represents a number specifying the shifted number of slots (slot offset number). Therefore, it is the case that correlation values P (0, 0) to P (63, 14) are stored in the memory.

[0059] Scrambling code group detecting unit 72c calculates the maximum (largest) value P_{max} (L, M) among the thus calculated power addition values P (I, m).

[0060] The value L obtained in this manner represents the scrambling code group number to which the scrambling code necessary for descrambling the frame belongs, and M represents slot offset number to the head of the frame.

[0061] The scrambling code group number L and slot offset number M detected in this manner are applied to control unit 74.

[0062] The third stage processed by scrambling code detecting unit 73 will be described in the following. In the third stage, scrambling code detecting unit 73 performs a process for the purpose of identifying the scrambling code used at the time of transmission by the base station. Such a third stage process will be described more specifically in the following.

[0063] Correlation processing unit 73a of scrambling code detecting unit 73 first receives from control unit 74, a signal indicating the timing of the head position of the frame based on the slot offset number detected in the second stage process described above, calculates 8 different correlation values with all of 8 different scrambling codes belonging to the scrambling code group number identified in the second stage for each frame, and stores the resulting values in a memory, not shown, in scrambling code specifying unit 73c.

[0064] Scrambling code specifying unit 73c detects the maximum correlation value from 8 correlation values obtained in the above described manner, and determines whether the detected maximum value exceeds a prescribed threshold value. When it exceeds, the scrambling code as the base for calculating the maximum correlation value is identified as the scrambling code for descrambling the frame, and identification information is applied to control unit 74. When the detected maximum correlation value does not exceed the threshold value, control unit 74 determines that identification of the scrambling code is impossible, and the process is repeated starting from the detection of slot

timing of the first stage.

[0065] The information is applied to despreading unit 66 of receiver 65 of the mobile station, and by the identified scrambling code, the received signal frame is descrambled.

[0066] In the conventional method of cell search described above, the scrambling code can be identified for the first time when the process of the third stage is completed, that is, whether cell search is successful or not is determined for the first time at the end of the third stage processing.

[0067] In the wireless transmission path, propagation environment changes with time, and the signal level may fluctuate significantly slot by slot. In such a reception environment, it becomes difficult to calculate accurate correlation values and to specify the scrambling code group in the second stage particularly, which may lead to a failure in identification of the scrambling code. For example, it is possible that, because of fluctuation of the received signal level, a strong correlation value is obtained for a specific slot, resulting in detection of an erroneous scrambling code group.

[0068] When identification of the scrambling code fails as described above, it is necessary to repeat the process from the first stage. Therefore, the process of cell search takes a very long time period. This eventually results in increased power consumption of the receiver of the mobile station.

SUMMARY OF THE INVENTION

[0069] Therefore, an object of the present invention is to provide a frame timing detecting circuit, a frame timing detecting method, a cell search apparatus and a portable wireless terminal using the cell search apparatus, which reduces time necessary for cell search and prevents increase in power consumption of the mobile station (portable wireless terminal) by improving detection accuracy in the second stage of cell search.

[0070] The present invention provides a frame timing detecting circuit detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the frame timing detecting circuit including: slot correlation value calculating means for calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots; first storing means for storing the plurality of slot correlation values of respective ones of the plurality of slots; frame correlation value calculating means for calculating a plurality of frame correlation values, by shifting the slots and at every shifting, accumulating the plurality of slot correlation values corresponding to respective ones of a plurality of combinations of the synchronization codes, among the plurality of slot correlation values of respective ones of the plurality of slots stored in the first storing means; maximum value detecting means for detecting, by shifting the slots, a maximum value among the plurality of frame correlation values calculated at every shift; second storing means for storing, by shifting the slots, the maximum value of the frame correlation value detected at every shift; determining means for detecting the largest value among the frame correlation values stored in the second storing means, and for generating information defining a frame start timing based on corresponding shift of the slots; and deviation calculating means for performing deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first storing means, and/or for performing deviation process on the plurality of frame correlation values calculated by the frame correlation value calculating means and applying a result to the second storing means.

[0071] Preferably, the plurality of different scrambling codes are classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; and the determining means generates information for specifying any of the plurality of combinations of the synchronization codes corresponding to the largest one of the frame correlation values stored in the second storing means, and specifying a group of the scrambling codes corresponding to the specified combination of the synchronization codes.

[0072] According to another aspect, the present invention provides a frame timing detecting circuit detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the frame timing detecting circuit including: slot correlation value calculating means for calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots; first maximum value detecting means for detecting a maximum value among the plurality of slot correlation values of respective ones of the plurality of slots and for specifying combinations of synchronization codes correlated to the detected respective maximum values; first storing means for storing the specified combinations of synchronization codes; synchronization code matching means for successively comparing, by shifting the slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in the first storing means with the plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of syn-

chronization codes corresponding to the plurality of slots among the plurality of combinations of the synchronization codes; second storing means storing, by shifting the slots, a value representing the specified highest correlation specified at every shift; determining means for detecting a largest value among the values representing the highest correlation stored in the second storing means, and for generating information defining a frame start timing based on the corresponding shift of the slot; and deviation calculating means for performing a deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first maximum value detecting means.

[0073] Preferably, the first maximum value detecting means detects a largest value of the plurality of slot correlation values of respective ones of the plurality of slots to specify a first combination of the synchronization codes corresponding to the detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to the detected respective values; the first storing means stores the specified first and second combinations of the synchronization codes; and the synchronization code matching means successively compares, by shifting the slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in the first storing means with the plurality of combinations of the synchronization codes, to specify one of the plurality of combinations of the synchronization codes that has highest correlation with the first and second combinations of the synchronization codes.

[0074] Preferably, the plurality of different scrambling codes are classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; and the determining means generates information for specifying any of the plurality of combinations of the synchronization codes corresponding to the largest one of the values representing the highest correlation stored in the second storing means and for specifying a group of the scrambling codes corresponding to the specified combination of the synchronization codes.

[0075] According to a still another aspect, the present invention provides a frame timing detecting method detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the method including the steps of: calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots; storing the plurality of slot correlation values of respective ones of the plurality of slots; calculating a plurality of frame correlation values, by shifting the slots and at every shifting, accumulating the plurality of slot correlation values corresponding to respective ones of a plurality of combinations of the synchronization codes, among the plurality of slot correlation values of respective ones of the stored plurality of slots; detecting, by shifting the slots, a maximum value among the plurality of frame correlation values calculated at every shift; storing, by shifting the slots, the maximum value of the frame correlation value detected at every shift; detecting the largest value among the stored frame correlation values, and generating information defining a frame start timing based on corresponding shift of the slots; and performing deviation processing on the plurality of slot correlation values to be stored and/or performing deviation processing on the plurality of frame correlation values to be stored.

[0076] Preferably, the plurality of different scrambling codes are classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; and the step of generating the frame start timing generates information for specifying any of the plurality of combinations of the synchronization codes corresponding to the largest one of the stored frame correlation values, and specifying a group of the scrambling codes corresponding to the specified combination of the synchronization codes.

[0077] According to a still further aspect, the present invention provides a frame timing detecting method detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the method including the steps of: calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots; detecting a maximum value among the plurality of slot correlation values of respective ones of the plurality of slots and specifying combinations of synchronization codes correlated to the detected respective maximum values; storing the specified combinations of synchronization codes; successively comparing, by shifting the slots and at every shifting, the combinations of synchronization codes corresponding to the stored shifted plurality of slots with the plurality of combinations of synchronization codes, and specifying one having highest correlation with the combination of synchronization codes corresponding to the plurality of slots among the plurality of combinations of the synchronization codes; storing, by shifting the slots, a value representing the specified highest correlation specified at every shift; detecting a largest value among the stored values representing the highest correlation, and generating information defining a frame start timing based on the corresponding shift of

the slot; and performing a deviation processing on the plurality of slot correlation values as objects of the maximum value detection.

[0078] More preferably, the step of detecting a maximum value among the plurality of slot correlation values detects a largest value of the plurality of slot correlation values of respective ones of the plurality of slots to specify a first combination of the synchronization codes corresponding to the detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to the detected respective values; the step of storing the specified combinations of synchronization codes stores the specified first and second combinations of the synchronization codes; and the step of specifying one having highest correlation successively compares, by shifting the slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the stored plurality of shifted slots with the plurality of combinations of the synchronization codes, to specify one of the plurality of combinations of the synchronization codes that has highest correlation with the first and second combinations of the synchronization codes.

[0079] More preferably, the plurality of different scrambling codes are classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; and the step of generating information defining a frame start timing generates information for specifying any of the plurality of combinations of the synchronization codes corresponding to the largest one of the stored values representing the highest correlation, and specifying a group of the scrambling codes corresponding to the specified combination of the synchronization codes.

[0080] According to a still further aspect, the present invention provides a cell search apparatus detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, and specifying the scrambling codes, the plurality of different scrambling codes being classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes, the cell search apparatus including: slot timing detecting means for detecting a start timing of the plurality of slots; and frame timing detecting means for detecting the start timing of the frame and for specifying a scrambling code group to which the scrambling code belongs; wherein the frame timing detecting means includes slot correlation value calculating means for calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots the start timing of which has been detected; first storing means for storing the plurality of slot correlation values of respective ones of the plurality of slots; frame correlation value calculating means for calculating a plurality of frame correlation values, by shifting the slots and at every shifting, accumulating the plurality of slot correlation values corresponding to respective ones of a plurality of combinations of the synchronization codes, among the plurality of slot correlation values of respective ones of the plurality of slots stored in the first storing means; maximum value detecting means for detecting, by shifting the slots, a maximum value among the plurality of frame correlation values calculated at every shift; second storing means for storing, by shifting the slots, the maximum value of the frame correlation value detected at every shift; determining means for detecting the largest value among the frame correlation values stored in the second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of the plurality of combinations of corresponding synchronization codes and specifying a group of scrambling codes corresponding to the specified combination of synchronization codes; and deviation calculating means for performing deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first storing means, and/or for performing deviation process on the plurality of frame correlation values calculated by the frame correlation value calculating means and applying a result to the second storing means; the cell search apparatus further including scrambling code detecting means for specifying the scrambling code among the specified group of synchronization codes.

[0081] According to a still further aspect, the present invention provides a cell search apparatus detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, and specifying the scrambling codes, the plurality of different scrambling codes being classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes, the cell search apparatus including: slot timing detecting means for detecting a start timing of the plurality of slots; and frame timing detecting means for detecting the start timing of the frame and for specifying a scrambling code group to which the scrambling code belongs; wherein the' frame timing detecting means includes slot correlation value calculating means for calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots the start timing of which has been detected, first maximum value detecting means for de-

tecting a maximum value among the plurality of slot correlation values of respective ones of the plurality of slots and for specifying combinations of synchronization codes correlated to the detected respective maximum values, first storing means for storing the specified combinations of synchronization codes, synchronization code matching means for successively comparing, by shifting the slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in the first storing means with the plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of synchronization codes corresponding to the plurality of slots among the plurality of combinations of the synchronization codes, second storing means storing, by shifting the slots, a value representing the specified highest correlation specified at every shift, determining means for detecting a largest value among the values representing the highest correlation stored in the second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of the plurality of combinations of corresponding synchronization codes and specifying a group of scrambling codes corresponding to the specified combination of synchronization codes, and deviation calculating means for performing a deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first maximum value detecting means; the cell search apparatus further including scrambling code detecting means for specifying the scrambling code among the specified group of synchronization codes.

[0082] Preferably, the first maximum value detecting means detects a largest value of the plurality of slot correlation values of respective ones of the plurality of slots to specify a first combination of the synchronization codes corresponding to the detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to the detected respective values; the first storing means stores the specified first and second combinations of the synchronization codes; and the synchronization code matching means successively compares, by shifting the slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in the first storing means with the plurality of combinations of the synchronization codes, to specify one of the plurality of combinations of the synchronization codes that has highest correlation with the first and second combinations of the synchronization codes.

[0083] According to a still further aspect, the present invention provides a portable wireless terminal for digital wireless communication, including: modem means for reception for demodulating received digital data; and signal processing means for processing and outputting the signal received by the modem means for reception; wherein the received digital data is a received signal sequence divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the plurality of different scrambling codes being classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; the modem means for reception includes a cell search apparatus for detecting a start timing of the received signal sequence and specifying the scrambling code; the cell search apparatus includes slot timing detecting means for detecting a start timing of the plurality of slots, and frame timing detecting means for detecting the start timing of the frame and for specifying a scrambling code group to which the scrambling code belongs; the frame timing detecting means includes slot correlation value calculating means for calculating a plurality of slot. correlation values using the plurality of different synchronization codes for each of the plurality of slots the start timing of which has been detected, first storing means for storing the plurality of slot correlation values of respective ones of the plurality of slots, frame correlation value calculating means for calculating a plurality of frame correlation values, by shifting the slots and at every shifting, accumulating the plurality of slot correlation values corresponding to respective ones of a plurality of combinations of the synchronization codes, among the plurality of slot correlation values of respective ones of the plurality of slots stored in the first storing means, maximum value detecting means for detecting, by shifting the slots, a maximum value among the plurality of frame correlation values calculated at every shift, second storing means for storing, by shifting the slots, the maximum value of the frame correlation value detected at every shift, determining means for detecting the largest value among the frame correlation values stored in the second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of the plurality of combinations of corresponding synchronization codes and specifying a group of scrambling codes corresponding to the specified combination of synchronization codes, and deviation calculating means for performing deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first storing means, and/or for performing deviation process on the plurality of frame correlation values calculated by the frame correlation value calculating means and applying a result to the second storing means; and the cell search apparatus further includes scrambling code detecting means for specifying the scrambling code among the specified group of synchronization codes.

[0084] According to a still further aspect, the present

invention provides a portable wireless terminal for digital wireless communication, including: modem means for reception for demodulating received digital data; and signal processing means for processing and outputting the signal received by the modem means for reception; wherein the received digital data is a received signal sequence divided into frames each formed of a plurality of slots, each of the plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of the frames having been spread by any of a plurality of different scrambling codes of long periods, the plurality of different scrambling codes being classified into a plurality of groups corresponding to the plurality of combinations of the synchronization codes; the modem means for reception includes a cell search. apparatus for detecting a start timing of the received signal sequence and specifying the scrambling code; the cell search apparatus includes slot timing detecting means for detecting a start timing of the plurality of slots, and frame timing detecting means for detecting the start timing of the frame and for specifying a scrambling code group to which the scrambling code belongs; the frame timing detecting means includes slot correlation value calculating means for calculating a plurality of slot correlation values using the plurality of different synchronization codes for each of the plurality of slots the start timing of which has been detected, first maximum value detecting means for detecting a maximum value among the plurality of slot correlation values of respective ones of the plurality of slots and for specifying combinations of synchronization codes correlated to the detected respective maximum values, first storing means for storing the specified combinations of synchronization codes, synchronization code matching means for successively comparing, by shifting the slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in the first storing means with the plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of synchronization codes corresponding to the plurality of slots among the plurality of combinations of the synchronization codes, second storing means storing, by shifting the slots, a value representing the specified highest correlation specified at every shift, determining means for detecting a largest value among the values representing the highest correlation stored in the second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of the plurality of combinations of corresponding synchronization codes and specifying a group of scrambling codes corresponding to the specified combination of synchronization codes, and deviation calculating means for performing a deviation processing on the plurality of slot correlation values calculated by the slot correlation value calculating means and applying a result to the first maximum value detecting means; and the cell search apparatus further includes scrambling code detecting means for specifying the scrambling code among the specified group of synchronization codes.

[0085] Preferably, the first maximum value detecting means detects a largest value of the plurality of slot correlation values of respective ones of the plurality of slots to specify a first combination of the synchronization codes corresponding to the detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to the detected respective values; the first storing means stores the specified first and second combinations of the synchronization codes; and the synchronization code matching means successively compares, by shifting the slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in the first storing means with the plurality of combinations of the synchronization codes, to specify one of the plurality of combinations of the synchronization codes that has highest correlation with the first and second combinations of the synchronization codes.

[0086] Therefore, according to the present invention, a deviation of a plurality of slot correlation values calculated by a plurality of different synchronization codes for each slot is calculated and/or deviation of a plurality of frame correlation values calculated after reception of 1 frame is calculated, for subsequent processing. Therefore, even when propagation environment of the wireless communication path changes with time with the reception signal level significantly changing slot by slot, the process of detecting frame timing (scrambling code group) of the succeeding stage can be performed accurately with the influence of such fluctuation removed, and therefore, accuracy of cell search by the mobile station (portable wireless terminal) can be improved.

[0087] Further, in the present invention, process is performed based on two synchronization code numbers that correspond to largest and the second largest values among a plurality of correlation values calculated slot by slot, and therefore circuit scale and the amount of calculation can be reduced.

[0088] Further, in the present invention, process is performed considering not only the correlation of the synchronization code number of the sequence corresponding to the maximum correlation values of respective slots but also the correlation of the synchronization code number of the sequence corresponding to the second largest correlation values. Therefore, even when the sequence of the maximum values and the sequence of the second maximum values are inverted by some cause such as noise, it is possible to accurately detect the frame timing and the scrambling code group.

[0089] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunc-

tion with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0090]

Fig. 1 is a schematic block diagram showing an overall configuration of a portable wireless terminal of digital wireless communication, to which the frame timing detecting circuit and the cell search apparatus of the present invention are applied.

Fig. 2 is a schematic block diagram representing a frame timing detecting unit in accordance with the first embodiment of the present invention.

Fig. 3 is a block diagram representing a configuration of a deviation calculating unit 104.

Fig. 4 shows an arrangement of deviations of the correlation values stored in storing unit 105.

Fig. 5 is a block diagram representing a configuration of a frame correlation value calculating unit 106.

Fig. 6 is a block diagram representing a configuration of a deviation calculating unit 107.

Fig. 7 is a flow chart representing a process when an operation of frame timing detecting unit 100 shown in Fig. 2 is executed in a software manner using a DSP.

Fig. 8 is a functional block diagram showing a modification of the first embodiment shown in Fig. 2.

Fig. 9 is a functional block diagram showing a further modification of the first embodiment shown in Fig. 2.

Fig. 10 is a schematic block diagram representing the frame timing detecting unit in accordance with the second embodiment of the present invention.

Fig. 11 shows an arrangement of synchronization code numbers stored in storing unit 506.

Fig. 12 is a block diagram representing a configuration of a synchronization code matching unit 507.

Fig. 13 is a flow chart showing a process when an operation of frame timing detecting unit 200 shown in Fig. 10 is executed in a software manner using a DSP.

Fig. 14 is a schematic block diagram showing basic configuration of a transmitter and a receiver in a direct sequence spread spectrum communication system in accordance with the CDMA system.

Fig. 15 is a functional block diagram representing a configuration of a cell search unit 70 performing the cell search process in a mobile station of a base stations asynchronous system.

Fig. 16 is a schematic diagram representing a signal format of a control channel in accordance with 3GPP standard.

Fig. 17 is a table representing combinations of second synchronization code numbers allocated corresponding to slots of 1 frame, for every scrambling code group number.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0091] Embodiments of the present invention will now be described in detail with reference to the figures. In the figures, the same or corresponding portions are denoted by the same reference characters and description thereof will not be repeated.

[0092] Fig. 1 is a schematic block diagram showing the overall configuration of the portable wireless terminal for digital radio communication to which the frame timing detecting circuit and the cell search apparatus of the present invention are applied.

[0093] The portable wireless terminal shown in Fig. 1 is generally constituted of an antenna 1, a radio processing unit 2, a baseband processing unit 3, a sound input/output device 4 formed of a microphone and a speaker, an external memory 5, and a display/input device 6 formed of an LCD and keys.

[0094] In particular, baseband processing unit 3 includes a modem 3a, a channel codec 3b, a DSP 3c, a CPU 3d, an internal memory 3e, an external interface 3f and an internal bus 3g.

[0095] A radiowave signal from a base station, not shown, and received by antenna 1 is converted to a baseband signal by radio processing unit 2, and applied to baseband processing unit 3.

[0096] In baseband processing unit 3, the received signal is demodulated by modem 3a, decoded by channel codec 3b and supplied to DSP 3c. DSP 3c performs data processing of the received signal, drives the speaker of sound input/output device 4 and converts the received signal into sound.

[0097] The sound input by means of the microphone of sound input/output device 4 undergoes data processing by DSP 3c to be supplied to channel codec 3b. Channel codec 3b encodes the supplied sound signal and provides the signal to modem 3a, and modem 3a modulates the transmission signal thus provided and supplies the modulated signal to radio processing unit 2. Radio processing unit 2 performs radio processing on the transmission signal and transmits the signal to a base station, not shown, via antenna 1.

[0098] Modem 3a, channel codec 3b and DSP 3c are connected via internal bus 3g to CPU 3d, internal memory 3e and external interface 3f. CPU 3d controls the entire operation of the portable wireless terminal of Fig. 1 in accordance with a program stored in internal memory 3e. External interface 3f functions as an interface with external memory 5 and displays/input device 6.

First Embodiment

[0099] Fig. 2 is a schematic block diagram representing the frame timing detecting circuit in accordance with the first embodiment of the present invention applied to the portable wireless terminal shown in Fig. 1. The circuit shown in Fig. 2 corresponds to frame timing detect-

ing unit 72 of the second stage of cell search unit 70 shown in Fig. 15, and it will be referred to as frame timing detecting unit 100 hereinafter. In the first embodiment of the present invention, the first and third stages of cell search are the same as the first stage performed by the slot timing detecting unit 71 and the third stage performed by the scrambling code detecting unit 73 shown in Fig. 15, and therefore, descriptions of the first and third stages will not be repeated.

[0100] More specifically, to the slot timing detecting unit 71 of the first stage and the scrambling code detecting unit 73 of the third stage shown in Fig. 15, the frame timing detecting unit 100 in accordance with the first embodiment of the present invention is added as the second stage, whereby the cell search unit (cell search apparatus) in accordance with the first embodiment of the present invention is implemented.

[0101] Here, it is assumed that despreading unit 66 (and cell search unit 70 of Fig. 15 included therein) as well as demodulating unit 67 of receiver 65 of the mobile station shown in Fig. 14 generally constitute the modem unit (not shown) for reception in modem 3a of baseband processing unit 3 of the portable wireless terminal shown in Fig. 1, and frame timing detecting unit 100 (included in cell search unit 70 of Fig. 15) of the first embodiment shown in Fig. 2 is also included in the modem unit for reception.

[0102] In the embodiments described in the following, as in the prior art example described above, it is assumed that 1 frame of the transmission signal from the base station includes 15 slots, 512 different types of scrambling codes are used for scrambling on the base station side, the 512 different scrambling codes are classified into 64 scrambling code groups (each corresponding to 8 different types of scrambling codes), and the synchronization channel is arranged at the head symbol position of every slot (each slot being formed of a plurality of symbols) constituting the frame.

[0103] The frame timing detecting unit 100 shown in Fig. 2 includes a slot correlation value calculating unit 101, an absolute value sum calculating unit 102, a deviation calculating unit 104, a storing unit 105, a frame correlation value calculating unit 106, a deviation calculating unit 107, a maximum value detecting unit 108, a storing unit 109, a determining unit 110, and a control unit 103.

[0104] The process of the second stage of cell search in accordance with the first embodiment shown in Fig. 2 will be described. The second stage process is, as in the prior art described above, to detect the timing of the boundary frame by frame, and to detect to which of 64 scrambling code groups the scrambling code used for scrambling the frame belongs.

[0105] Control unit 103 mainly controls operation timings of various portions of frame timing detecting unit 100. Control unit 103 receives a slot timing signal indicative of the timing of the head symbol of each slot applied from slot timing detecting unit 71 of the first stage shown in Fig. 15 and sets a flag signal which assumes, for example, "1" only in the head symbol section of each slot and "0" in other sections.

[0106] While the flag signal of "1" is set, control unit 103 turns and keeps on the slot correlation value calculating unit 101, absolute value sum calculating unit 102, deviation calculating unit 104 and storing unit 105.

[0107] Further, control unit 103 set a flag signal that assumes "1" when 15 slots of a slot timing signal are received, that is, after 1 frame is received, and assumes "0" in other sections.

[0108] While the flag signal of "1" is set, control unit 103 turns and keeps on the frame correlation value calculating unit 106, deviation calculation unit 107, maximum value detecting unit 108, storing unit 109 and determining unit 110.

[0109] Slot correlation value calculating unit 101 calculates 16 correlation values between each of I phase component and Q phase component of the received signal and 16 different second synchronization codes (SSC_i: i = 1, 2, ..., 16) in accordance with an instruction from control unit 13 that receives the slot timing signal, and applies 16 correlation values SCI_i corresponding to the I phase component and 16 correlation values SCQ_i corresponding to the Q phase component, to absolute value sum calculating unit 102. In the following description, the second synchronization code will be simply referred to as the synchronization code (which is distinguished from the first synchronization code of the first stage shown in Fig. 15).

[0110] The absolute value sum calculating unit 102 converts 16 correlation values input separately for each of I phase and Q phase to absolute values, add pairs (SCI_i, SCQ_i) of correlation values of I phase and Q phase to each other that have been subjected to correlation value calculation with common synchronization code SSC_i, and provides 16 correlation values SC_i.

[0111] Thus provided 16 correlation value outputs SC_i of absolute value sum calculating unit 102 are applied to deviation calculating unit 104. Fig. 3 is a block diagram representing the configuration of deviation calculating unit 104.

[0112] Referring to Fig. 3, deviation calculating unit 104 includes an average value calculating unit 201 and a difference calculating unit 202. Deviation calculating unit 104 calculates an average value of input 16 correlation values SC_i at average value calculating unit 201, and calculates difference from the average value of each of 16 correlation values SC_i at difference calculating unit 202 so as to convert the values to 16 deviations. The deviation outputs SCD_i are stored successively slot by slot in storing unit 105.

[0113] Fig. 4 shows an arrangement of the deviations of the correlation values stored in this manner in storing unit 105. Deviations $SCD_{i,j}$ are stored in correspondence with synchronization code numbers i that specify respective ones of 16 different synchronization codes (ordinate) used for calculating the correlation values,

and slot numbers j that specify respective ones of 15 slots #1 to #15 (abscissa) constituting 1 frame.

[0114] The process from slot correlation value calculating unit 101 to storing unit 105 described above is performed for every symbol section of each slot, after the start of processing by frame timing detecting unit 100. When all correlation value deviations SCD_l, j of 15 slots corresponding to 1 frame are stored in storing unit 105 as shown in the table of Fig. 4, control unit 103 starts processing of the next stage, so that processing by frame correlation value calculating unit 16 and circuits of the succeeding stages start.

[0115] In this stage, the above described process by slot correlation value calculating unit 101, absolute value sum calculating unit 102, deviation calculating unit 104 and storing unit 105 may be stopped.

[0116] Fig. 5 is a block diagram representing a configuration of frame correlation value calculating unit 106. Referring to Fig. 5, frame correlation value calculating unit 106 includes an integrating unit 301, a memory 302 and a memory control unit 303.

[0117] Memory 302 stores a table of combinations formed by (second) synchronization code numbers allocated corresponding to the slots of 1 frame for each of the scrambling code group numbers shown in Fig. 17. Integrating unit 301 selectively accumulates correlation value deviations corresponding to respective slots stored as shown in Fig. 4 in storing unit 105, based on the table of Fig. 17 held in memory 302, in accordance with the combinations of synchronization codes determined for each of the scrambling code groups, and calculates 64 different frame correlation values FC_k (k = 1, 2, ..., 64) that correspond to 64 scrambling code groups, respectively.

[0118] More specifically, memory control unit 303 operates such that a synchronization code number is read from the combination table of Fig. 17 stored in memory 302 and a corresponding correlation value deviation is read from storing unit 105 based thereon to be applied to integrating unit 301.

[0119] The process for calculating the frame correlation value is executed for every one of 64 scrambling code groups and every one of 15 slots. The basic process, however, is common to all the scrambling code groups. Therefore, the process will be described in detail taking a scrambling code group No. 1 as an example.

[0120] Refer to the row of Group 1 in the table of Fig. 17. For slot #1, the first synchronization code SSC_1 is designated as the spreading code. Therefore, the value stored in the first column and first row of the arrangement table of correlation value deviations shown in Fig. 4, that is, the correlation value deviation SCD_1, 1 calculated using the first synchronization code SSC_1 when slot #1 is received, is read from storing unit 105 and applied to integrating unit 301.

[0121] Next, in slot #2, first synchronization code SSC_1 is designated as the spreading code, in the similar manner. Therefore, the value stored in the second column, first row of the arrangement table of correlation value deviations, that is, the correlation value deviation SCD_1, 2 calculated using the first synchronization code SSC_1 when slot #2 is received, is read from storing unit 105 and applied to integrating unit 301, where it is accumulated to the previously read correlation value deviation SCD_1, 1.

[0122] Thereafter, reading and accumulation of the correlation value deviations are repeated in the similar manner up to slot #15, and the value finally obtained by accumulation at integrating unit 305 is output as a frame correlation value FC_1 corresponding to scrambling code group No. 1, from frame correlation value calculating unit 106.

[0123] Though scrambling code group No. 1 has been described, frame correlation values FC_2 to FC_{64} are obtained by the similar processing for remaining scrambling code group Nos. 2 to 64, and output from frame correlation value calculating unit 106.

[0124] Thus obtained 64 frame correlation values FC_k (k = 1, 2, ..., 64) are applied to deviation calculating unit 107 of the succeeding stage.

[0125] Fig. 6 is a block diagram representing a configuration of deviation calculating unit 107. Referring to Fig. 6, deviation calculating unit 107 includes an average value calculating unit 401 and a difference calculating unit 402. Deviation calculating unit 107 calculates an average value of input 64 frame correlation values FC_k at average value calculating unit 401, and calculates a difference between each of 64 frame correlation values FC_k and the average value at difference calculating unit 402, and converts the differences to 64 deviations. The deviation output FCD_k is input to maximum value detecting unit 108 of the succeeding stage.

[0126] Maximum value detecting unit 108 detects a maximum (largest) value FCD_l of the applied 64 deviations FCD_k, and the maximum value FCD_1 and the corresponding scrambling code group number 1 are stored in storing unit 109 of the succeeding stage.

[0127] Here, on the mobile station side, the frame start timing (frame boundary) of the transmission signal is actually unknown, and therefore, it is not known how many slots the slot for starting the process of accumulating the correlation value for each slot at the frame correlation value calculating unit 106 is shifted from the frame timing (slot offset number).

[0128] Therefore, it is further necessary to detect the maximum correlation value deviation $FCD_{l,m}$ (m = 0, 1, ..., 14) and the corresponding scrambling code group number l_m, when the slot offset number is 1, 2, ... 14.

[0129] Frame correlation value calculating unit 106, deviation calculating unit 107 and maximum value detecting unit 108 detect the maximum correlation value deviation $FCD_{l,m}$ and scrambling code group number l_m for each of 15 cases with the slot offset number being 1 to 14, while shifting slot by slot, and the results are stored in storing unit 109. Namely, storing unit 109 stores a total of 15 sets of maximum correlation value

deviation and the corresponding scrambling code group number.

[0130] Determining unit 110 detects the maximum one of 15 maximum correlation value deviations $FCD_{l,m}$ stored in storing unit 109, and compares the detected value with a prescribed threshold value. When it is determined to be exceeding the threshold value, determining unit 110 applies the corresponding scrambling code group number 1 and the slot offset number m for determining the frame timing, to scrambling code detecting unit 73 of the third stage of cell search, shown in Fig. 15.

[0131] When it is determined to be not exceeding the threshold value, determining unit 110 applies a signal indicative of scrambling code group detection failure to control unit 103. Receiving this signal, control unit 103 executes the above described control for detecting the frame timing again, from the reception slot thereafter.

[0132] In case of scrambling code group detection failure, the number of repetition of the above described control is variable. Detection accuracy, however, is not always improved when the number of repetition is large. Repetition up to three times may be desirable. When the scrambling code group is still not detected, the process returns to the first stage of cell search, to start again from the detection of slot timing by slot timing detecting unit 71 of Fig. 15.

[0133] Fig. 7 is a flow chart representing a process when the operation of frame timing detecting unit 100 shown in Fig. 2 is executed in a software manner, using a DSP.

[0134] Referring to Fig. 7, in step S1, when it is determined by the slot timing signal from slot timing detecting unit 71 of Fig. 15 that the timing is in the slot head symbol section, slot correlation values are calculated for I phase component and Q phase component of the received signal in step S2.

[0135] Next, in step S3, absolute value sum SC_i of these two is calculated, in step S4, the slot correlation value deviation SCD_i is calculated, and the result is stored in storing unit 105 in step S5.

[0136] Thereafter, until calculation of slot correlation value deviations of 15 slots corresponding to 1 frame is complete in step S6, the process of steps S1 to S6 is repeated.

[0137] When it is determined that all the slot correlation value deviations have been calculated for 1 frame (15 slots) in step S6, in step S7, the slot correlation value deviations stored in storing unit 105 (see arrangement table of Fig. 4) are accumulated, based on the combination table of synchronization codes of Fig. 17 stored in memory 302, and frame correlation value sum FC_k is calculated for each of 64 scrambling code groups.

[0138] Thereafter, in step S8, deviations FCD_k of frame correlation value sums are calculated, and in step S9, the maximum value $FCD_{l,m}$ is detected therefrom, and stored in storing unit 109 in step S10.

[0139] Until the slot offset number m reaches 14 in step S11, the process of steps S7 to S11 is repeated.

[0140] When it is determined in step S11 that the maximum value $FCD_{l,m}$ has been detected for every slot offset number, the maximum $FCD_{l,m}$ is determined in step S12, and whether the value exceeds a prescribed threshold value or not is determined in step S13.

[0141] When it is determined in step S13 that the threshold value is exceeded, the corresponding scrambling code group number and the slot offset number are determined in step S14. When it is determined in step S13 that the threshold value is not exceeded, the process of steps S1 to S13 is repeated, up to a prescribed number of times, until the threshold value is exceeded.

[0142] In the process of specifying the frame timing and the scrambling code group in accordance with the first embodiment shown in the functional block diagram of Fig. 2 and the flow chart of Fig. 7, deviation of 16 slot correlation values calculated by 16 different synchronization codes is taken for each slot and used for the subsequent processing. Therefore, even when propagation environment in the wireless transmission path fluctuates with time and the received signal level changes significantly slot by slot, the frame correlation value can be calculated exactly in the succeeding stage with the influence of fluctuation removed, and hence accuracy in detecting the frame timing and the scrambling code group can be improved.

[0143] Further, in the first embodiment, as deviation of 64 frame correlation values calculated after reception of 1 frame (15 slots) is taken and used for subsequent processing, variation among correlation values with respect to a prescribed threshold can be removed, enabling more accurate detection of the frame timing and the scrambling code group.

[0144] Though deviation of slot correlation value and deviation of frame correlation value are both calculated in the first embodiment, calculation of only one of these may be sufficient to attain satisfactory results.

[0145] Fig. 8 is a functional block diagram representing a modification of the first embodiment shown in Fig. 2. In this example, deviation calculating unit 107 of the succeeding stage of Figs 2 is omitted. Even when the deviation calculating unit 107 of the succeeding stage is omitted, accuracy in detecting the frame timing and the scrambling code group can sufficiently be improved, when variation among slot correlation values is removed by the deviation calculating unit 104 of the preceding stage.

[0146] Fig. 9 is a functional block diagram representing a further modification of the first embodiment shown in Fig. 2. In this example, the deviation calculating unit 104 of the preceding stage of Fig. 2 is omitted. Even when the deviation calculating unit 104 of the preceding stage is omitted, accuracy in detecting the frame timing and the scrambling code group can sufficiently be improved when variation among frame correlation values is removed by the deviation calculating unit 107 of the succeeding stage.

Second Embodiment

[0147] Fig. 10 is a schematic block diagram representing a frame timing detecting unit in accordance with the second embodiment of the present invention, which is applied to a portable wireless terminal shown in Fig. 1. The circuit shown in Fig. 10 corresponds to the frame timing detecting unit 72 of the second stage of cell search unit 70 shown in Fig. 15, and the circuit will be hereinafter referred to as frame timing detecting unit 200. In the second embodiment also, the first stage and the third stage of cell search are the same as the first stage performed by the slot timing detecting unit 71 and the third stage performed by the scrambling code detecting unit 73 shown in Fig. 15, and therefore descriptions of the first and third stages will not be repeated.

[0148] More specifically, to the slot timing detecting unit 71 of the first stage and the scrambling code detecting unit 73 of the third stage shown in Fig. 15, the frame timing detecting unit 200 in accordance with the second embodiment is added as the second stage, whereby the cell search unit (cell search apparatus) in accordance with the second embodiment is implemented.

[0149] Frame timing detecting unit 200 shown in Fig. 10 includes a slot correlation value calculating unit 501, an absolute value sum calculating unit 502, a deviation calculating unit 504, a maximum value detecting unit 505, a storing unit 506, a synchronization code matching unit 507, a maximum value detecting unit 508, a storing unit 509, a determining unit 510 and a control unit 503.

[0150] The process of the second stage of cell search by the second embodiment shown in Fig. 10 will be described in the following. As in the prior art described above, the second stage processing is to detect the timing of the boundary of each frame, and to detect to which of 64 scrambling code groups the scrambling code used for scrambling the frame belongs.

[0151] Slot correlation value calculating unit 501, absolute value sum calculating unit 502 and deviation calculating unit 504 correspond to slot correlation value calculating unit 101, absolute value sum calculating unit 102 and deviation calculating unit 104 of the first embodiment shown in Fig. 2. Therefore, description thereof will not be repeated.

[0152] Maximum value detecting unit 505 detects the maximum one among 16 correlation value deviations SCD_i (i = 1, 2, ..., 16) output slot by slot from deviation calculating unit 504, and stores the corresponding synchronization code number successively in storing unit 506, slot by slot.

[0153] Maximum value detecting unit 505 further detects the maximum one among the remaining 15 correlation value deviations, that is, the second largest correlation value deviation among 16 correlation value deviations slot by slot, and stores the corresponding synchronization code number successively in memory unit 506 slot by slot.

[0154] As a result, a combination of synchronization code numbers (sequence A) from which maximum correlation value deviations are obtained for respective ones of 15 slots and a combination of synchronization code numbers (sequence B) from which second largest correlation value deviations are obtained for respective ones of 15 slots are stored, in correspondence with the slot numbers, in storing unit 506.

[0155] Fig. 11 is a table of arrangement representing a state in which sequences A and B are stored in correspondence with slot numbers #1 to #15. Referring to Fig. 11, synchronization code number is represented by i, slot number by I, the synchronization code number column of sequence A by $A1_i$, I, and the synchronization code number column of sequence B is represented by $A2_i$,I.

[0156] After receiving 15 slots corresponding to 1 frame, it follows that a total of 30 (15 × 2) synchronization code numbers of sequences A and B are stored in storing unit 506. Thereafter, the control proceeds to the process by synchronization code matching unit 507, maximum value detecting unit 508, storing unit 509 and determining unit 510. After entrance of this process, processes by slot correlation value calculating unit 501 to storing unit 506 may be stopped.

[0157] Fig. 12 is a block diagram representing the configuration of synchronization code matching unit 507 of Fig. 10. Referring to Fig. 12, synchronization code matching unit 507 includes matching number counters 601 and 602, a memory 603, a memory control unit 604 and an addition unit 605.

[0158] Memory 603 stores a table of combinations of (second) synchronization code numbers that are allocated corresponding to the slots of 1 frame, for each scrambling code group number shown in Fig. 17.

[0159] Memory control unit 604 reads a corresponding combination of synchronization code numbers for each of the scrambling code group numbers from the table shown in Fig. 17 held in memory 603, and commonly applies the read combination to one input of each of matching number counters 601 and 602.

[0160] To the other input of matching number counter 601, the synchronization code number A1i, I of sequence A is applied from storing unit 506, and to the other input of matching number counter 602, synchronization code number $A2_i$, I of sequence B is applied from storing unit 506.

[0161] Matching number counter 601 compares each of the combinations of synchronization code numbers corresponding to 64 scrambling code groups of the table shown in Fig. 17 with the combination of synchronization code numbers of sequence A, and for each of 64 scrambling code groups, counts the number of slots $M1_j$, of which synchronization code numbers matched. Here, j represents the scrambling code group number = 1, 2, ..., 64.

[0162] The matching number counter 602 compares each of the combinations of synchronization code numbers corresponding to 64 scrambling code groups of the

table shown in Fig. 17 with the combination of synchronization code numbers of sequence B, and counts the number of slots $M2_j$ of which synchronization code numbers matched.

[0163] The elements (synchronization code numbers) of sequences A and B of an arbitrary slot number do not match each other. Further, there is the relation of $0 \leq M1_j + M2_j \leq 15$.

[0164] Thereafter, for each of scrambling code group numbers, the count value $M1_j$ of matching number counter 601 is weighted with a coefficient α, the count value $M2_j$ of matching number counter 602 is weighted with the coefficient of β, and the total sum M_j is given by adding unit 605 as $M_j = \alpha \cdot M1_j + \beta \cdot M2_j$. Such a calculation is executed corresponding to every one of 64 scrambling code groups.

[0165] The maximum value detecting unit 508 detects the value M_l that is the largest among 64 values M_j input from synchronization code matching unit 507 in this manner, and stores the detected value together with the scrambling code group number I corresponding to the maximum value, in storing unit 509.

[0166] Here, actually, on the mobile station side, the start timing (frame boundary) of the frame of the transmission signal is unknown, and therefore, how many slots the start slot of the process for counting matching numbers of synchronization code numbers slot by slot by the synchronization code matching unit 507 is shifted from the frame timing (slot offset number) is unknown.

[0167] Therefore, it is further necessary to detect the maximum value $M_{l,m}$, (m = 0, 1, ..., 14) and the corresponding scrambling code group number l_m, when the slot offset number is 1, 2, ... 14.

[0168] Synchronization code matching unit 507 and maximum value detecting unit 509 detect the maximum value $M_{l,m}$, and scrambling code group number l_m for each of 15 cases with the slot offset number being 1 to 14, while shifting slot by slot, and stores the detected values in storing unit 509. More specifically, storing unit 509 stores a total of 15 sets of maximum values $M_{l,m}$ and corresponding scrambling code group numbers l_m.

[0169] Determining unit 510 detects the largest one of 15 maximum values $M_{l,m}$ stored in storing unit 509, and compares the detected value with a prescribed threshold value. When it is determined to be exceeding the threshold value, determining unit 510 applies the corresponding scrambling code group number I and the slot offset number m for determining the frame timing, to scrambling code detecting unit 73 of the third stage of cell search shown in Fig. 15.

[0170] When it is determined to be not exceeding the threshold value, determining unit 510 applies a signal indicating scrambling code group detection failure to control unit 503. Upon reception of this signal, control unit 503 executes the above described control for detecting the frame timing again, from the following reception slot.

[0171] In case of scrambling code group detection failure, the number of repetition of the above described control is variable. Detection accuracy, however, is not always improved when the number of repetition is large. Repetition up to three times may be desirable. When the scrambling code group is still not detected, the process returns to the first stage of cell search, to start again from the detection of slot timing by slot timing detecting unit 71 of Fig. 15.

[0172] Fig. 13 is a flow chart representing a process when the operation of frame timing detecting unit 200 shown in Fig. 10 is executed in a software manner, using a DSP.

[0173] Referring to Fig. 13, in step S21, when it is determined by the slot timing signal from slot timing detecting unit 71 of Fig. 15 that the timing is in the slot head symbol section, slot correlation values are calculated for I phase component and Q phase component of the received signal in step S22.

[0174] Next, in step S23, absolute value sum SC_i of these two is calculated, and in step S24, the slot correlation value deviation SCD_i is calculated.

[0175] In step S25, the synchronization code number which results in the maximum value among the calculated slot correlation value deviations is detected, and in step S26, the synchronization code number that results in the second largest value is detected. The detected synchronization code numbers are stored in storing unit 506 in step S27.

[0176] In step S28, until the synchronization code sequence A providing the maximum correlation value deviation and the synchronization code sequence B providing the second largest value for 15 slots corresponding to 1 frame are obtained, the process from steps S21 to S28 is repeated.

[0177] When it is determined in step S28 that all the synchronization codes for sequences A and B are obtained for 1 frame (15 slots), the number of matching of synchronization code numbers of sequences A and B is counted for each of 64 scrambling code groups of the combination table of synchronization codes shown in Fig. 17 stored in memory 603, and the value $M_j = \alpha \cdot M1_j + \beta \cdot M2_j$ is calculated.

[0178] In step S30, the maximum value $M_{l,m}$ thereof is detected, and stored in storing unit 509 in step S31.

[0179] Until the slot offset number m reaches 14 in step S32, the process of steps S29 to S32 is repeated.

[0180] When it is determined in step S32 that the maximum value $M_{l,m}$ has been detected for every slot offset number, the maximum $M_{l,m}$ is determined in step S33, and whether the value exceeds a prescribed threshold value or not is determined in step S34.

[0181] When it is determined in step S34 that the threshold value is exceeded, the corresponding scrambling code group number and the slot offset number are determined in step S35. When it is determined in step S34 that the threshold value is not exceeded, the process of steps S21 to S34 is repeated, up to a prescribed times, until the threshold value is exceeded.

[0182] In the process of specifying the frame timing and the scrambling code group in accordance with the second embodiment shown in the functional block diagram of Fig. 10 and the flow chart of Fig. 13, deviation of 16 slot correlation values calculated by 16 different synchronization codes is taken for each slot and used for the subsequent processing. Therefore, even when propagation environment in the wireless transmission path fluctuates with time and the received signal level changes significantly slot by slot, the synchronization code matching process can be performed exactly in the succeeding stage with the influence of fluctuation removed, and hence accuracy in detecting the frame timing and the scrambling code group can be improved.

[0183] In the second embodiment, not only the number of matching of synchronization code numbers of sequence A corresponding to the maximum correlation value deviation of respective slots but also the number of matching of synchronization code numbers of sequence B corresponding to the second largest correlation value deviation are considered for processing. It is possible that the sequence of the maximum value and the sequence of the second maximum value are inverted by noise or other cause, and the above described process is to ensure accurate detection of frame timing and scrambling code group even in such a situation.

[0184] In the second embodiment, two synchronization code numbers that correspond to the largest and the second largest values of 16 correlation value deviations calculated for each slot are used for the processing, and therefore, capacity of storing unit 506 can be reduced, and the circuit scale of synchronization code matching unit 507 and succeeding stages as well as the amount of calculation can be reduced.

[0185] As described above, according to the present invention, the deviation of a plurality of slot correlation values calculated by a plurality of different synchronization codes for each slot of the received signal sequence is taken and/or deviation of a plurality of frame correlation values calculated after reception of 1 frame is taken and used for the subsequent processing. Therefore, even when propagation environment of wireless transmission path fluctuates with time and received signal levels changed significantly slot by slot, it is possible to accurately perform the process of detecting frame timing (and scrambling code group) of the succeeding stage with the influence of such fluctuation removed, and hence accuracy of cell search by the mobile station (portable wireless terminal) can be increased.

[0186] As a result, the time necessary for cell search can be reduced, and the power consumption of the portable wireless terminal is reduced.

[0187] Further, in the present invention, process is performed based on two synchronization code numbers corresponding to the largest and the second largest values among a plurality of correlation values calculated for each slot, and therefore, circuit scale and the amount of calculation can be reduced.

[0188] Further, in the present invention not only the correlation of synchronization code numbers of the sequence corresponding to the maximum correlation value but also correlation of the synchronization code numbers of the sequence corresponding to the second largest correlation value of respective slots are considered for processing. Therefore, even when the sequence of the largest value and the sequence of the second largest value should be inverted by noise or some other cause, it is possible to accurately detect the frame timing and the scrambling code group.

[0189] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A frame timing detecting circuit (100) detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said frame timing detecting circuit comprising:

   slot correlation value calculating means (101) for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots;
   first storing means (105) for storing said plurality of slot correlation values of respective ones of said plurality of slots;
   frame correlation value calculating means (106) for calculating a plurality of frame correlation values, by shifting said slots and at every shifting, accumulating said plurality of slot correlation values corresponding to respective ones of a plurality of combinations of said synchronization codes, among said plurality of slot correlation values of respective ones of said plurality of slots stored in said first storing means;
   maximum value detecting means (108) for detecting, by shifting said slots, a maximum value among said plurality of frame correlation values calculated at every shift;
   second storing means (109) for storing, by shifting said slots, the maximum value of said frame correlation value detected at every shift;
   determining means (110) for detecting the larg-

est value among said frame correlation values stored in said second storing means, and for generating information defining a frame start timing based on corresponding shift of the slots; and

deviation calculating means (104, 107) for performing deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first storing means, and/or for performing deviation process on said plurality of frame correlation values calculated by said frame correlation value calculating means and applying a result to said second storing means.

2. The frame timing detecting circuit according to claim 1, wherein

said plurality of different scrambling codes are classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes; and

said determining means generates information for specifying any of said plurality of combinations of the synchronization codes corresponding to the largest one of said frame correlation values stored in said second storing means, and specifying a group of the scrambling codes corresponding to said specified combination of the synchronization codes.

3. A frame timing detecting circuit (200) detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said frame timing detecting circuit comprising:

slot correlation value calculating means (501) for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots;

first maximum value detecting means (505) for detecting a maximum value among said plurality of slot correlation values of respective ones of said plurality of slots and for specifying combinations of synchronization codes correlated to said detected respective maximum values;

first storing means (506) for storing said specified combinations of synchronization codes;

synchronization code matching means (507) for successively comparing, by shifting said slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in said first storing means with said plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of synchronization codes corresponding to said plurality of slots among the plurality of combinations of said synchronization codes;

second storing means (509) storing, by shifting said slots, a value representing said specified highest correlation specified at every shift;

determining means (510) for detecting a largest value among said values representing the highest correlation stored in said second storing means, and for generating information defining a frame start timing based on the corresponding shift of the slot; and

deviation calculating means (504) for performing a deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first maximum value detecting means.

4. The frame timing detecting circuit according to claim 3, wherein

said first maximum value detecting means detects a largest value of said plurality of slot correlation values of respective ones of said plurality of slots to specify a first combination of the synchronization codes corresponding to said detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to said detected respective values;

said first storing means stores said specified first and second combinations of the synchronization codes; and

said synchronization code matching means successively compares, by shifting said slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in said first storing means with said plurality of combinations of the synchronization codes, to specify one of said plurality of combinations of the synchronization codes that has highest correlation with said first and second combinations of said synchronization codes.

5. The frame timing detecting circuit according to claim 3 or 4, wherein

said plurality of different scrambling codes are classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes; and

said determining means generates information for specifying any of said plurality of combina-

tions of the synchronization codes corresponding to the largest one of said values representing the highest correlation stored in said second storing means and for specifying a group of the scrambling codes corresponding to said specified combination of the synchronization codes.

6. A frame timing detecting method detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said method comprising the steps of:

calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots;
storing said plurality of slot correlation values of respective ones of said plurality of slots;
calculating a plurality of frame correlation values, by shifting said slots and at every shifting, accumulating said plurality of slot correlation values corresponding to respective ones of a plurality of combinations of said synchronization codes, among said plurality of slot correlation values of respective ones of said stored plurality of slots;
detecting, by shifting said slots, a maximum value among said plurality of frame correlation values calculated at every shift;
storing, by shifting said slots, the maximum value of said frame correlation value detected at every shift;
detecting the largest value among said stored frame correlation values, and generating information defining a frame start timing based on corresponding shift of the slots; and
performing deviation processing on said plurality of slot correlation values to be stored and/or performing deviation processing on said plurality of frame correlation values to be stored.

7. The frame timing detecting method according to claim 6, wherein

said plurality of different scrambling codes are classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes; and

said step of generating said frame start timing generates information for specifying any of said plurality of combinations of the synchronization codes corresponding to the largest one of said stored frame correlation values, and specifying a group of the scrambling codes corresponding to said specified combination of the synchronization codes.

8. A frame timing detecting method detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said method comprising the steps of:

calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots;
detecting a maximum value among said plurality of slot correlation values of respective ones of said plurality of slots and specifying combinations of synchronization codes correlated to said detected respective maximum values;
storing said specified combinations of synchronization codes;
successively comparing, by shifting said slots and at every shifting, the combinations of synchronization codes corresponding to the stored shifted plurality of slots with said plurality of combinations of synchronization codes, and specifying one having highest correlation with the combination of synchronization codes corresponding to said plurality of slots among the plurality of combinations of said synchronization codes;
storing, by shifting said slots, a value representing said specified highest correlation specified at every shift;
detecting a largest value among said stored values representing the highest correlation, and generating information defining a frame start timing based on the corresponding shift of the slot; and
performing a deviation processing on said plurality of slot correlation values as objects of said maximum value detection.

9. A frame timing detecting method according to claim 8, wherein

said step of detecting a maximum value among said plurality of slot correlation values detects a largest value of said plurality of slot correlation values of respective ones of said plurality of slots to specify a first combination of the synchronization codes corresponding to said detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to said detected respective values;

said step of storing said specified combina-

tions of synchronization codes stores said specified first and second combinations of the synchronization codes; and

said step of specifying one having highest correlation successively compares, by shifting said slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the stored plurality of shifted slots with said plurality of combinations of the synchronization codes, to specify one of said plurality of combinations of the synchronization codes that has highest correlation with said first and second combinations of said synchronization codes.

10. The frame timing detecting method according to claim 8 or 9, wherein

said plurality of different scrambling codes are classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes; and

said step of generating information defining a frame start timing generates information for specifying any of said plurality of combinations of the synchronization codes corresponding to the largest one of said stored values representing the highest correlation, and specifying a group of the scrambling codes corresponding to said specified combination of the synchronization codes.

11. A cell search apparatus (70) detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, and specifying said scrambling codes, said plurality of different scrambling codes being classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes, said cell search apparatus comprising:

slot timing detecting means (71) for detecting a start timing of said plurality of slots; and

frame timing detecting means (100) for detecting the start timing of said frame and for specifying a scrambling code group to which said scrambling code belongs; wherein

said frame timing detecting means includes

slot correlation value calculating means (101) for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots said start timing of which has been detected;

first storing means (105) for storing said plurality of slot correlation values of respective ones of said plurality of slots;

frame correlation value calculating means (106) for calculating a plurality of frame correlation values, by shifting said slots and at every shifting, accumulating said plurality of slot correlation values corresponding to respective ones of a plurality of combinations of said synchronization codes, among said plurality of slot correlation values of respective ones of said plurality of slots stored in said first storing means;

maximum value detecting means (108) for detecting, by shifting said slots, a maximum value among said plurality of frame correlation values calculated at every shift;

second storing means (109) for storing, by shifting said slots, the maximum value of said frame correlation value detected at every shift;

determining means (110) for detecting the largest value among said frame correlation values stored in said second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of said plurality of combinations of corresponding said synchronization codes and specifying a group of scrambling codes corresponding to said specified combination of synchronization codes; and

deviation calculating means (104, 107) for performing deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first storing means, and/or for performing deviation process on said plurality of frame correlation values calculated by said frame correlation value calculating means and applying a result to said second storing means;

said cell search apparatus further comprising

scrambling code detecting means (73) for specifying said scrambling code among said specified group of synchronization codes.

12. A cell search apparatus (70) detecting a start timing of a frame of a received signal sequence, the received signal sequence being divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, and specifying said scrambling codes, said plurality of different scrambling codes being classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes, said cell search apparatus comprising:

slot timing detecting means (71) for detecting a start timing of said plurality of slots; and
frame timing detecting means (100) for detecting the start timing of said frame and for specifying a scrambling code group to which said scrambling code belongs; wherein
said frame timing detecting means includes
slot correlation value calculating means (501) for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots said start timing of which has been detected,
first maximum value detecting means (505) for detecting a maximum value among said plurality of slot correlation values of respective ones of said plurality of slots and for specifying combinations of synchronization codes correlated to said detected respective maximum values,
first storing means (506) for storing said specified combinations of synchronization codes,
synchronization code matching means (507) for successively comparing, by shifting said slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in said first storing means with said plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of synchronization codes corresponding to said plurality of slots among the plurality of combinations of said synchronization codes,
second storing means (509) storing, by shifting said slots, a value representing said specified highest correlation specified at every shift,
determining means (510) for detecting a largest value among said values representing the highest correlation stored in said second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of said plurality of combinations of corresponding said synchronization codes and specifying a group of scrambling codes corresponding to said specified combination of synchronization codes, and
deviation calculating means (504) for performing a deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first maximum value detecting means;
said cell search apparatus further comprising
scrambling code detecting means (73) for specifying said scrambling code among said specified group of synchronization codes.

13. The cell search apparatus according to claim 12, wherein

said first maximum value detecting means detects a largest value of said plurality of slot correlation values of respective ones of said plurality of slots to specify a first combination of the synchronization codes corresponding to said detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to said detected respective values;

said first storing means stores said specified first and second combinations of the synchronization codes; and

said synchronization code matching means successively compares, by shifting said slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in said first storing means with said plurality of combinations of the synchronization codes, to specify one of said plurality of combinations of the synchronization codes that has highest correlation with said first and second combinations of said synchronization codes.

14. A portable wireless terminal for digital wireless communication, comprising:

modem means (3a) for reception for demodulating received digital data; and
signal processing means (3b, 3c) for processing and outputting the signal received by said modem means for reception; wherein
said received digital data is a received signal sequence divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said plurality of different scrambling codes being classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes;
said modem means for reception includes a cell search apparatus (70) for detecting a start timing of said received signal sequence and specifying said scrambling code;
said cell search apparatus includes
slot timing detecting means (71) for detecting a start timing of said plurality of slots, and
frame timing detecting means (100) for detecting the start timing of said frame and for specifying a scrambling code group to which said scrambling code belongs;
said frame timing detecting means includes
slot correlation value calculating means (101)

for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots said start timing of which has been detected,
first storing means (105) for storing said plurality of slot correlation values of respective ones of said plurality of slots,
frame correlation value calculating means (106) for calculating a plurality of frame correlation values, by shifting said slots and at every shifting, accumulating said plurality of slot correlation values corresponding to respective ones of a plurality of combinations of said synchronization codes, among said plurality of slot correlation values of respective ones of said plurality of slots stored in said first storing means,
maximum value detecting means (108) for detecting, by shifting said slots, a maximum value among said plurality of frame correlation values calculated at every shift,
second storing means (109) for storing, by shifting said slots, the maximum value of said frame correlation value detected at every shift,
determining means (110) for detecting the largest value among said frame correlation values stored in said second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information specifying any of said plurality of combinations of corresponding said synchronization codes and specifying a group of scrambling codes corresponding to said specified combination of synchronization codes, and
deviation calculating means (104, 107) for performing deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first storing means, and/or for performing deviation process on said plurality of frame correlation values calculated by said frame correlation value calculating means and applying a result to said second storing means; and
said cell search apparatus further includes
scrambling code detecting means (73) for specifying said scrambling code among said specified group of synchronization codes.

15. A portable wireless terminal for digital wireless communication, comprising:

modem means (3a) for reception for demodulating received digital data; and
signal processing means (3b, 3c) for processing and outputting the signal received by said modem means for reception; wherein
said received digital data is a received signal sequence divided into frames each formed of a plurality of slots, each of said plurality of slots having been spread on a transmitting side by any of a plurality of combinations of a plurality of different synchronization codes of short periods, and each of said frames having been spread by any of a plurality of different scrambling codes of long periods, said plurality of different scrambling codes being classified into a plurality of groups corresponding to said plurality of combinations of the synchronization codes;
said modem means for reception includes a cell search apparatus (70) for detecting a start timing of said received signal sequence and specifying said scrambling code;
said cell search apparatus includes
slot timing detecting means (71) for detecting a start timing of said plurality of slots, and
frame timing detecting means (100) for detecting the start timing of said frame and for specifying a scrambling code group to which said scrambling code belongs;
said frame timing detecting means includes
slot correlation value calculating means (501) for calculating a plurality of slot correlation values using said plurality of different synchronization codes for each of said plurality of slots said start timing of which has been detected,
first maximum value detecting means (505) for detecting a maximum value among said plurality of slot correlation values of respective ones of said plurality of slots and for specifying combinations of synchronization codes correlated to said detected respective maximum values,
first storing means (506) for storing said specified combinations of synchronization codes,
synchronization code matching means (507) for successively comparing, by shifting said slots and at every shifting, the combinations of synchronization codes corresponding to the shifted plurality of slots stored in said first storing means with said plurality of combinations of synchronization codes, for specifying one having highest correlation with the combination of synchronization codes corresponding to said plurality of slots among the plurality of combinations of said synchronization codes,
second storing means (509) storing, by shifting said slots, a value representing said specified highest correlation specified at every shift,
determining means (510) for detecting a largest value among said values representing the highest correlation stored in said second storing means, for generating information defining a frame start timing based on corresponding shift of the slots, and for generating information

specifying any of said plurality of combinations of corresponding said synchronization codes and specifying a group of scrambling codes corresponding to said specified combination of synchronization codes, and

deviation calculating means (504) for performing a deviation processing on said plurality of slot correlation values calculated by said slot correlation value calculating means and applying a result to said first maximum value detecting means; and

said cell search apparatus further includes scrambling code detecting means (73) for specifying said scrambling code among said specified group of synchronization codes.

16. The portable wireless terminal according to claim 15, wherein

said first maximum value detecting means detects a largest value of said plurality of slot correlation values of respective ones of said plurality of slots to specify a first combination of the synchronization codes corresponding to said detected respective values, and detects a second largest value to specify a second combination of the synchronization codes corresponding to said detected respective values;

said first storing means stores said specified first and second combinations of the synchronization codes; and

said synchronization code matching means successively compares, by shifting said slots and at every shifting, each of the first and second combinations of the synchronization codes corresponding to the plurality of shifted slots stored in said first storing means with said plurality of combinations of the synchronization codes, to specify one of said plurality of combinations of the synchronization codes that has highest correlation with said first and second combinations of said synchronization codes.

FIG. 1

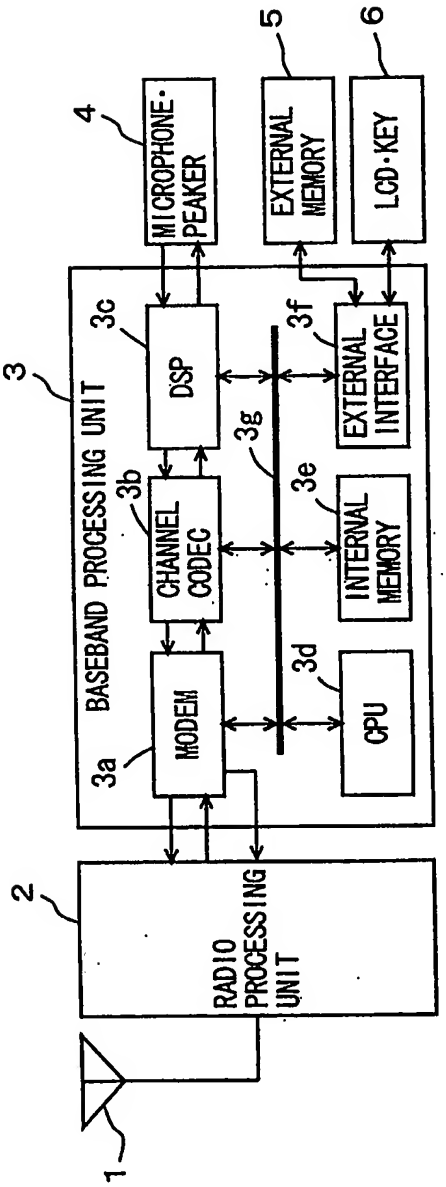
1
2
RADIO PROCESSING UNIT
3
BASEBAND PROCESSING UNIT
3a
MODEM
3b
CHANNEL CODEC
3c
DSP
3d
CPU
3e
INTERNAL MEMORY
3f
EXTERNAL INTERFACE
3g
4
MICROPHONE·PEAKER
5
EXTERNAL MEMORY
6
LCD·KEY

FIG. 2

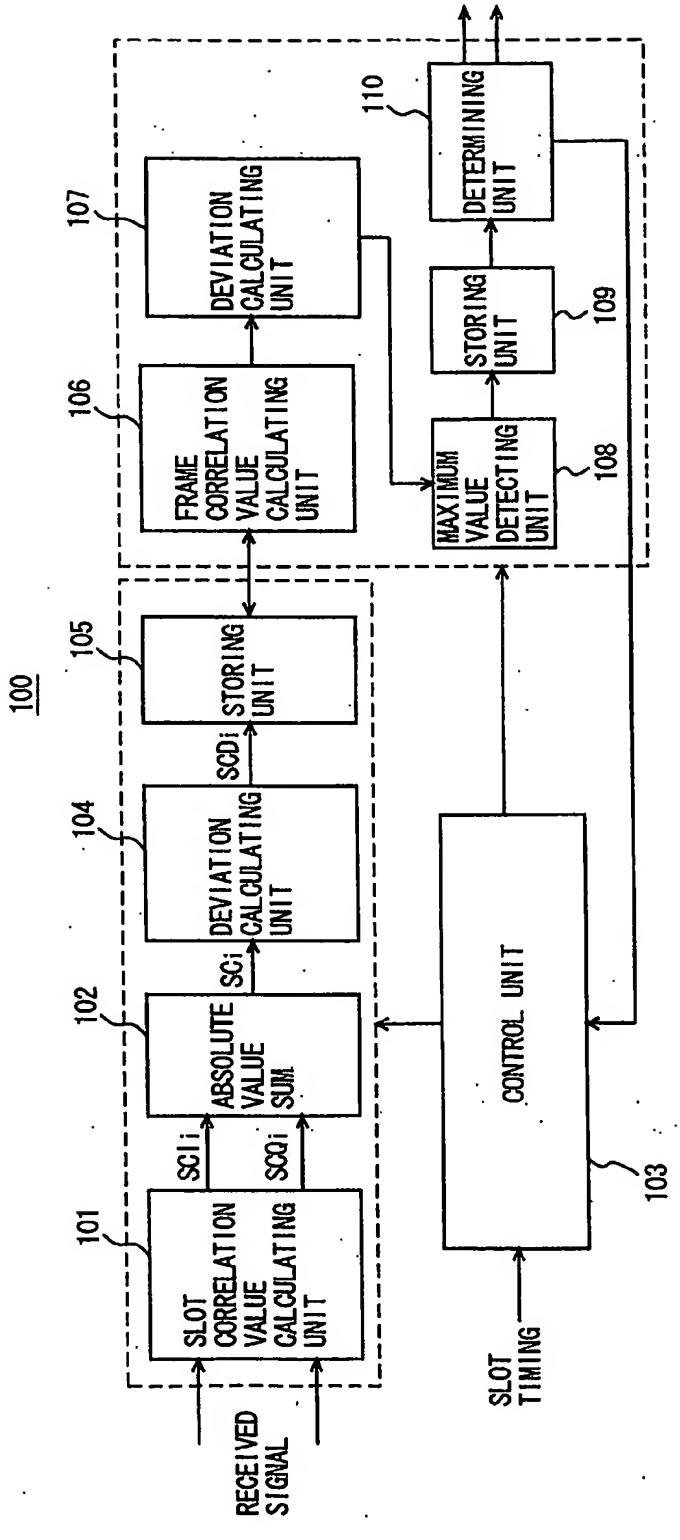
100
RECEIVED SIGNAL
SLOT TIMING
101
SLOT CORRELATION VALUE CALCULATING UNIT
102
ABSOLUTE VALUE SUM
103
CONTROL UNIT
104
DEVIATION CALCULATING UNIT
105
STORING UNIT
106
FRAME CORRELATION VALUE CALCULATING UNIT
107
DEVIATION CALCULATING UNIT
108
MAXIMUM VALUE DETECTING UNIT
109
STORING UNIT
110
DETERMINING UNIT
SCi
SCIi
SCQi
SCDi

FIG. 3

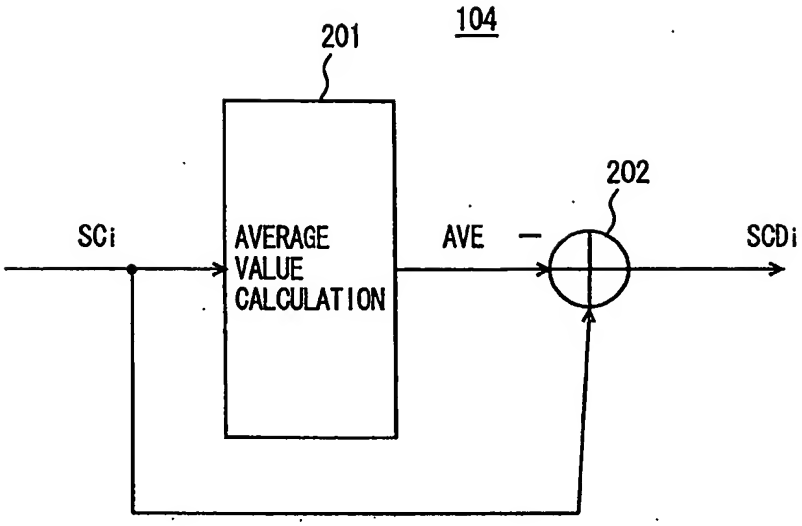
104
201
202
SCi
AVERAGE VALUE CALCULATION
AVE
SCDi

FIG. 6

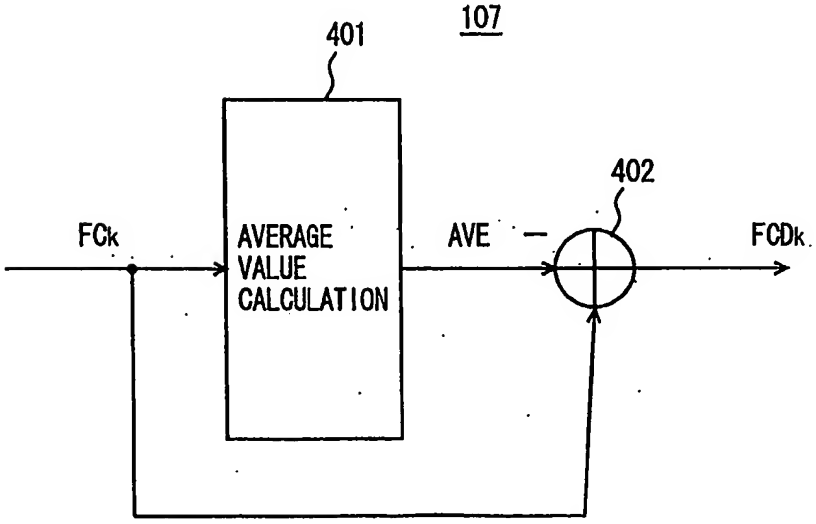
107
401
402
FCk
AVERAGE VALUE CALCULATION
AVE
FCDk

FIG. 4

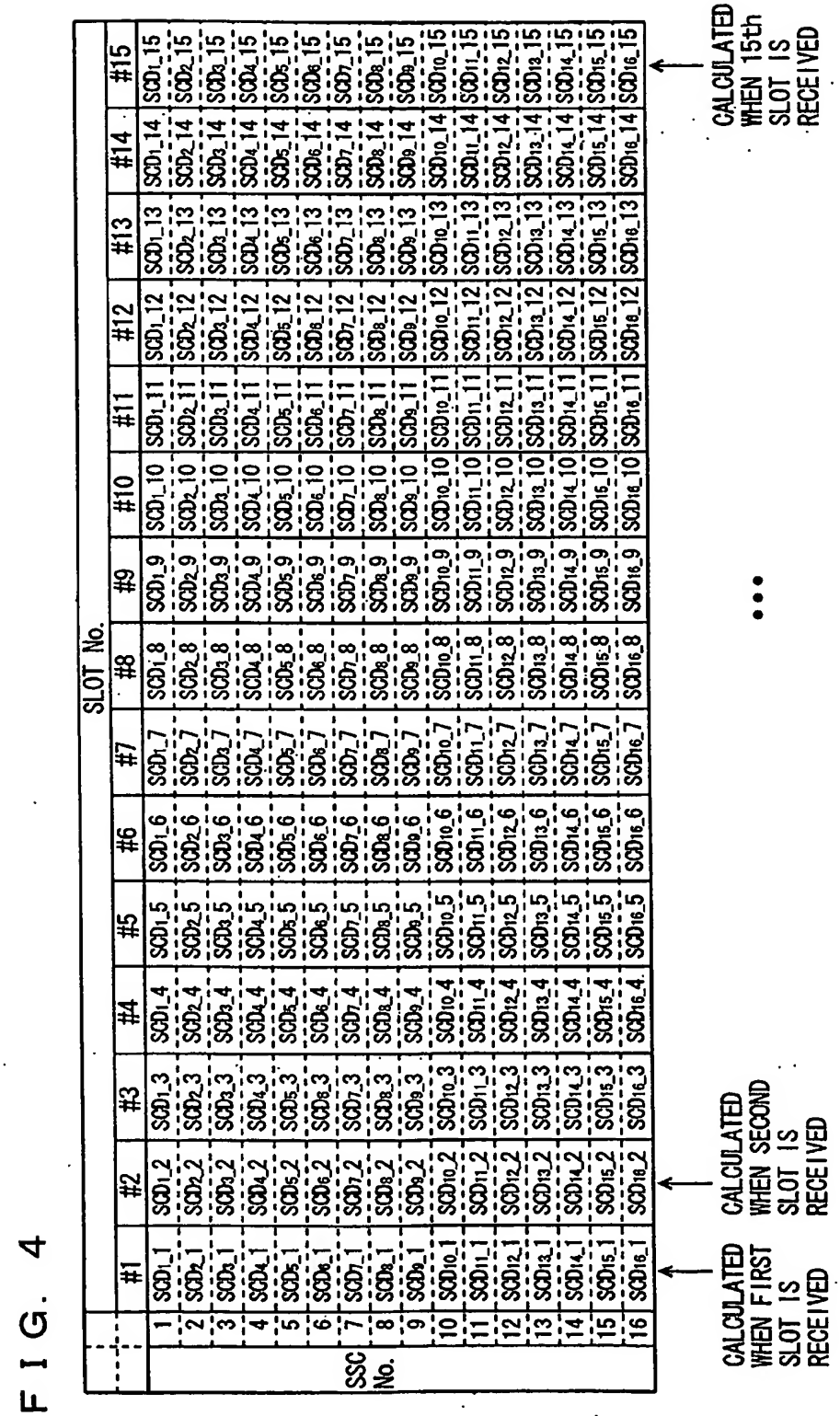
SLOT No.
#1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14 #15
SSC No.
1 SCD1_1 SCD1_2 SCD1_3 SCD1_4 SCD1_5 SCD1_6 SCD1_7 SCD1_8 SCD1_9 SCD1_10 SCD1_11 SCD1_12 SCD1_13 SCD1_14 SCD1_15
2 SCD2_1 SCD2_2 SCD2_3 SCD2_4 SCD2_5 SCD2_6 SCD2_7 SCD2_8 SCD2_9 SCD2_10 SCD2_11 SCD2_12 SCD2_13 SCD2_14 SCD2_15
3 SCD3_1 SCD3_2 SCD3_3 SCD3_4 SCD3_5 SCD3_6 SCD3_7 SCD3_8 SCD3_9 SCD3_10 SCD3_11 SCD3_12 SCD3_13 SCD3_14 SCD3_15
4 SCD4_1 SCD4_2 SCD4_3 SCD4_4 SCD4_5 SCD4_6 SCD4_7 SCD4_8 SCD4_9 SCD4_10 SCD4_11 SCD4_12 SCD4_13 SCD4_14 SCD4_15
5 SCD5_1 SCD5_2 SCD5_3 SCD5_4 SCD5_5 SCD5_6 SCD5_7 SCD5_8 SCD5_9 SCD5_10 SCD5_11 SCD5_12 SCD5_13 SCD5_14 SCD5_15
6 SCD6_1 SCD6_2 SCD6_3 SCD6_4 SCD6_5 SCD6_6 SCD6_7 SCD6_8 SCD6_9 SCD6_10 SCD6_11 SCD6_12 SCD6_13 SCD6_14 SCD6_15
7 SCD7_1 SCD7_2 SCD7_3 SCD7_4 SCD7_5 SCD7_6 SCD7_7 SCD7_8 SCD7_9 SCD7_10 SCD7_11 SCD7_12 SCD7_13 SCD7_14 SCD7_15
8 SCD8_1 SCD8_2 SCD8_3 SCD8_4 SCD8_5 SCD8_6 SCD8_7 SCD8_8 SCD8_9 SCD8_10 SCD8_11 SCD8_12 SCD8_13 SCD8_14 SCD8_15
9 SCD9_1 SCD9_2 SCD9_3 SCD9_4 SCD9_5 SCD9_6 SCD9_7 SCD9_8 SCD9_9 SCD9_10 SCD9_11 SCD9_12 SCD9_13 SCD9_14 SCD9_15
10 SCD10_1 SCD10_2 SCD10_3 SCD10_4 SCD10_5 SCD10_6 SCD10_7 SCD10_8 SCD10_9 SCD10_10 SCD10_11 SCD10_12 SCD10_13 SCD10_14 SCD10_15
11 SCD11_1 SCD11_2 SCD11_3 SCD11_4 SCD11_5 SCD11_6 SCD11_7 SCD11_8 SCD11_9 SCD11_10 SCD11_11 SCD11_12 SCD11_13 SCD11_14 SCD11_15
12 SCD12_1 SCD12_2 SCD12_3 SCD12_4 SCD12_5 SCD12_6 SCD12_7 SCD12_8 SCD12_9 SCD12_10 SCD12_11 SCD12_12 SCD12_13 SCD12_14 SCD12_15
13 SCD13_1 SCD13_2 SCD13_3 SCD13_4 SCD13_5 SCD13_6 SCD13_7 SCD13_8 SCD13_9 SCD13_10 SCD13_11 SCD13_12 SCD13_13 SCD13_14 SCD13_15
14 SCD14_1 SCD14_2 SCD14_3 SCD14_4 SCD14_5 SCD14_6 SCD14_7 SCD14_8 SCD14_9 SCD14_10 SCD14_11 SCD14_12 SCD14_13 SCD14_14 SCD14_15
15 SCD15_1 SCD15_2 SCD15_3 SCD15_4 SCD15_5 SCD15_6 SCD15_7 SCD15_8 SCD15_9 SCD16_10 SCD16_11 SCD15_12 SCD15_13 SCD15_14 SCD15_15
16 SCD16_1 SCD16_2 SCD16_3 SCD16_4 SCD16_5 SCD16_6 SCD16_7 SCD16_8 SCD16_9 SCD16_10 SCD16_11 SCD16_12 SCD16_13 SCD16_14 SCD16_15
CALCULATED WHEN FIRST SLOT IS RECEIVED
CALCULATED WHEN SECOND SLOT IS RECEIVED
CALCULATED WHEN 15th SLOT IS RECEIVED

FIG. 5

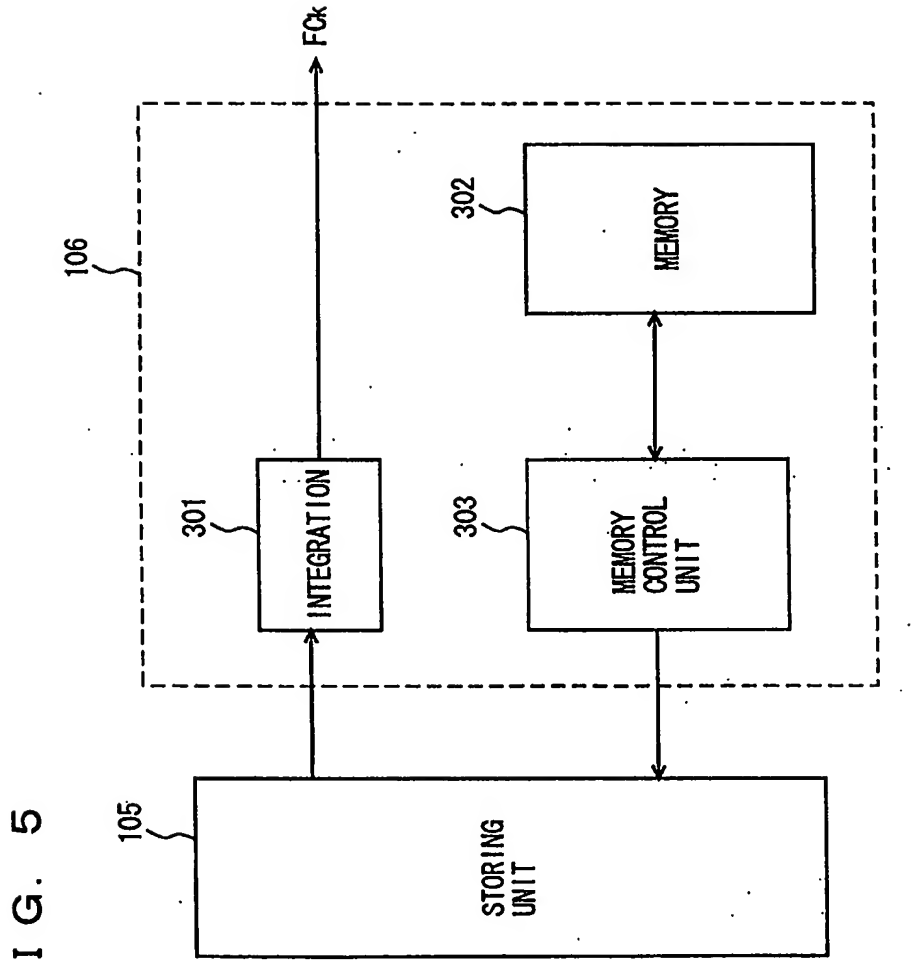
Fck
106
302
MEMORY
301
INTEGRATION
303
MEMORY CONTROL UNIT
105
STORING UNIT

FIG. 7

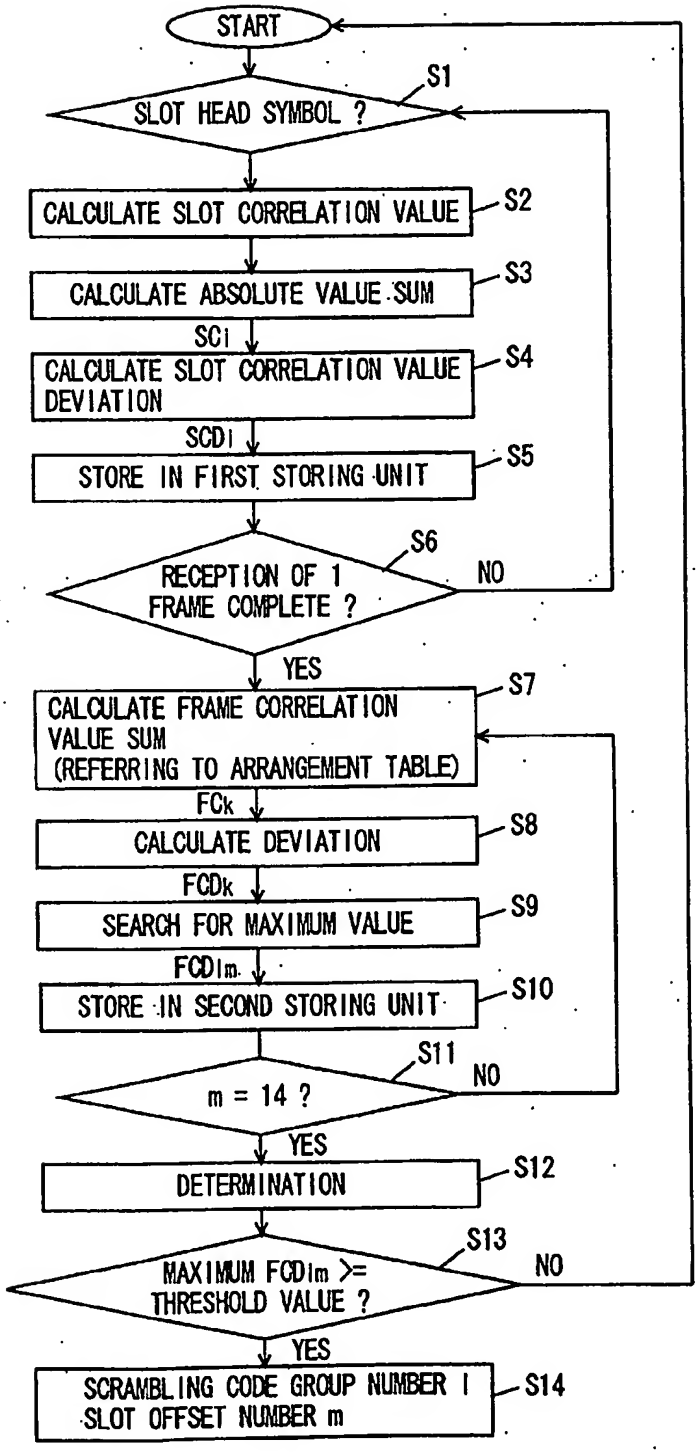
START
S1
SLOT HEAD SYMBOL ?
CALCULATE SLOT CORRELATION VALUE
S2
CALCULATE ABSOLUTE VALUE SUM
S3
SCi
CALCULATE SLOT CORRELATION VALUE DEVIATION
S4
SCDi
STORE IN FIRST STORING UNIT
S5
S6
RECEPTION OF 1 FRAME COMPLETE ?
NO
YES
CALCULATE FRAME CORRELATION VALUE SUM (REFERRING TO ARRANGEMENT TABLE)
S7
FCk
CALCULATE DEVIATION
S8
FCDk
SEARCH FOR MAXIMUM VALUE
S9
FCDIm
STORE IN SECOND STORING UNIT
S10
S11
m = 14 ?
NO
YES
DETERMINATION
S12
S13
MAXIMUM FCDIm >= THRESHOLD VALUE ?
NO
YES
SCRAMBLING CODE GROUP NUMBER I
SLOT OFFSET NUMBER m
S14

FIG. 8

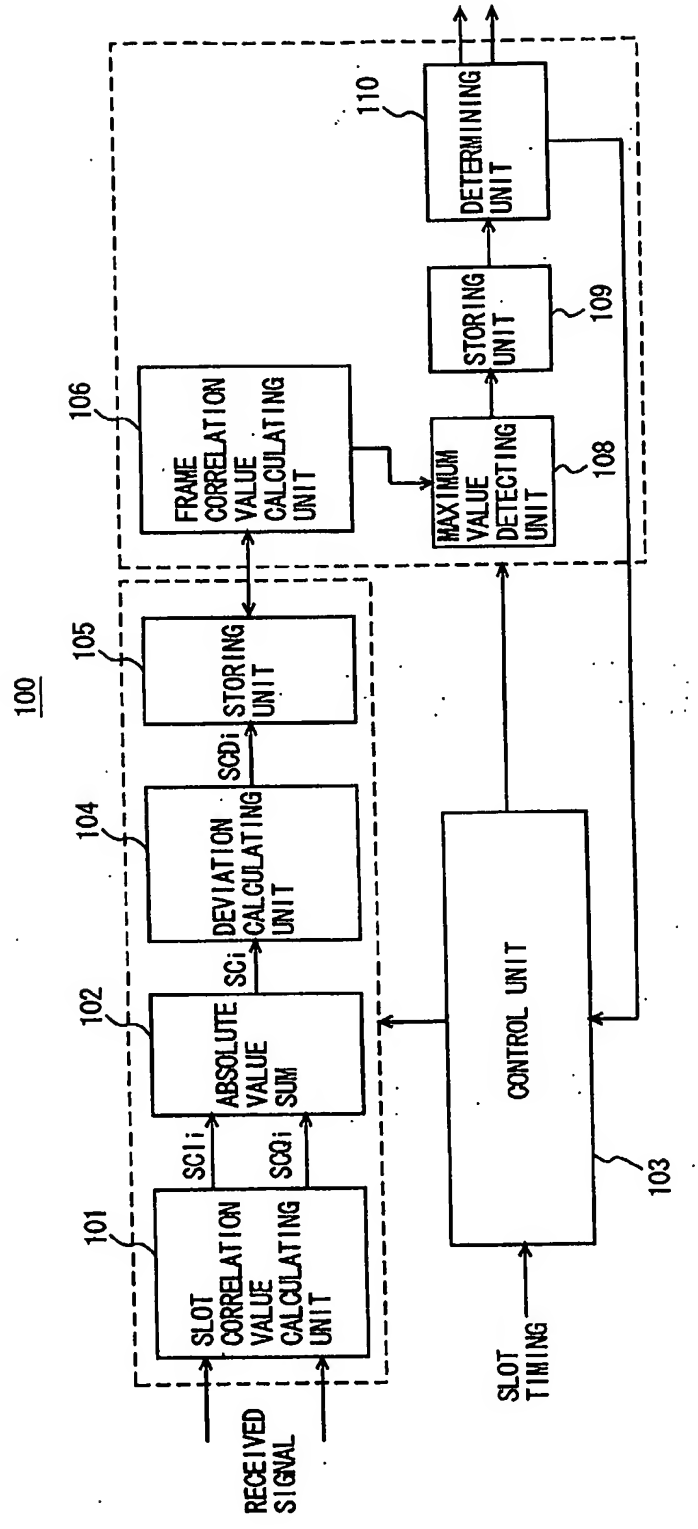
100
101
SLOT CORRELATION VALUE CALCULATING UNIT
SCIi
SCQi
102
ABSOLUTE VALUE SUM
SCi
104
DEVIATION CALCULATING UNIT
SCDi
105
STORING UNIT
106
FRAME CORRELATION VALUE CALCULATING UNIT
108
MAXIMUM VALUE DETECTING UNIT
109
STORING UNIT
110
DETERMINING UNIT
CONTROL UNIT
103
RECEIVED SIGNAL
SLOT TIMING

FIG. 9

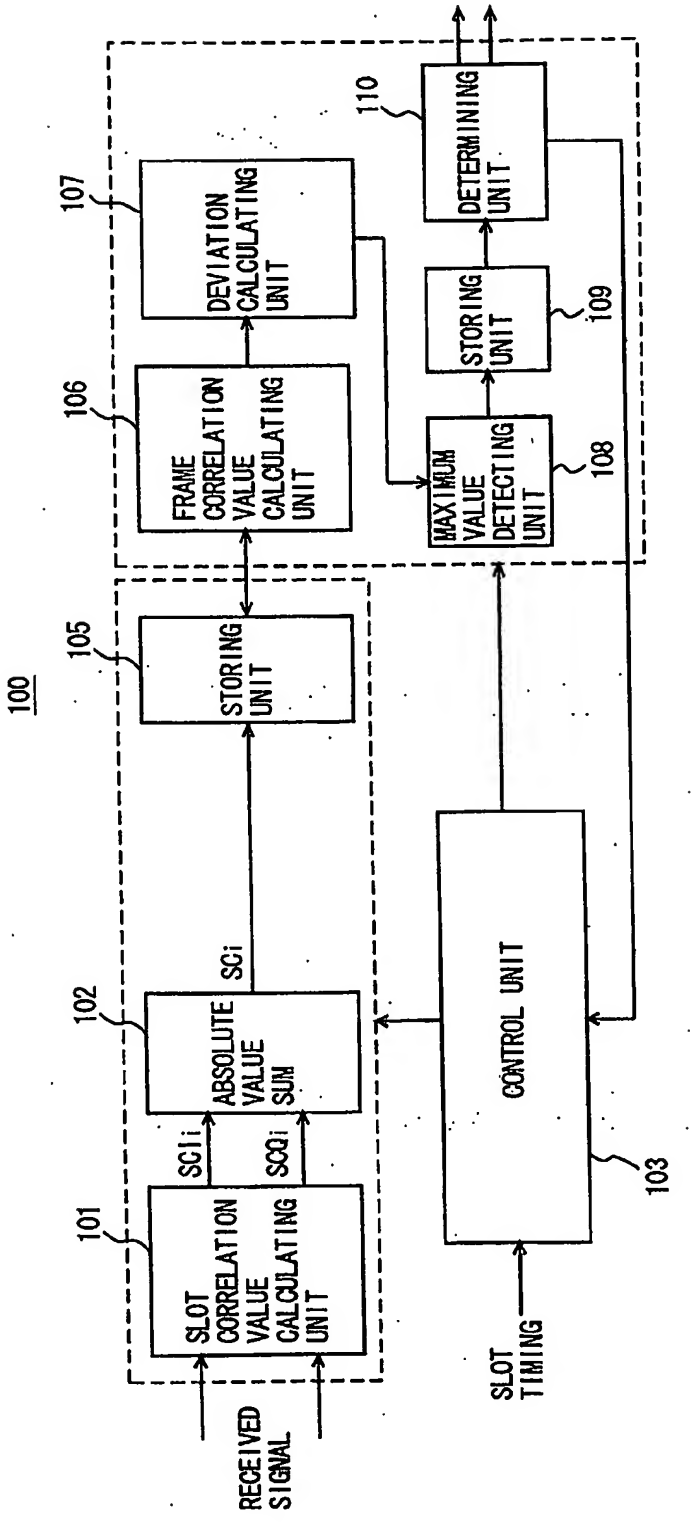
100
RECEIVED SIGNAL
SLOT TIMING
SLOT CORRELATION VALUE CALCULATING UNIT
101
SC1i
SC0i
ABSOLUTE VALUE SUM
102
SCi
STORING UNIT
105
FRAME CORRELATION VALUE CALCULATING UNIT
106
DEVIATION CALCULATING UNIT
107
MAXIMUM VALUE DETECTING UNIT
108
STORING UNIT
109
DETERMINING UNIT
110
CONTROL UNIT
103

FIG. 10

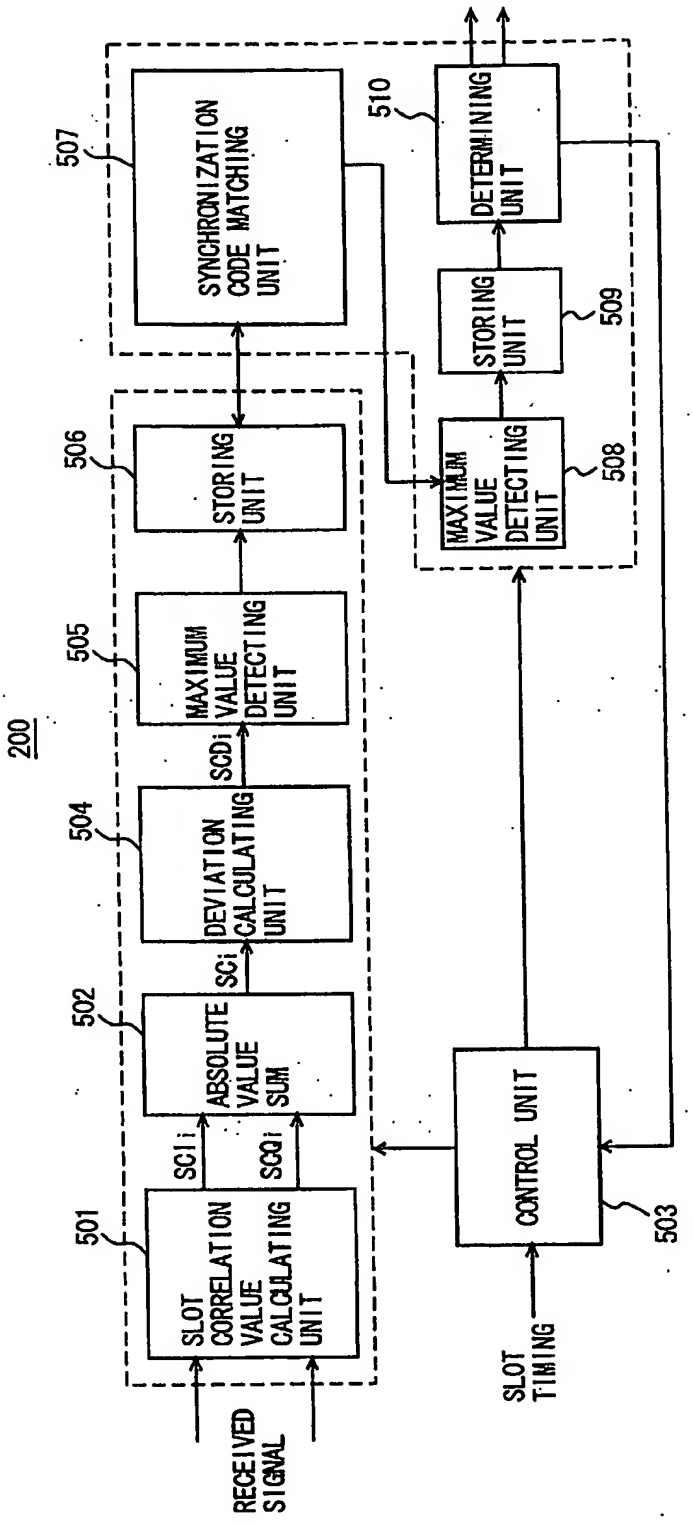
200
501
SLOT CORRELATION VALUE CALCULATING UNIT
502
ABSOLUTE VALUE SUM
504
DEVIATION CALCULATING UNIT
505
MAXIMUM VALUE DETECTING UNIT
506
STORING UNIT
507
SYNCHRONIZATION CODE MATCHING UNIT
503
CONTROL UNIT
508
MAXIMUM VALUE DETECTING UNIT
509
STORING UNIT
510
DETERMINING UNIT
SCIi
SCQi
SCi
SCDi
RECEIVED SIGNAL
SLOT TIMING

FIG. 11

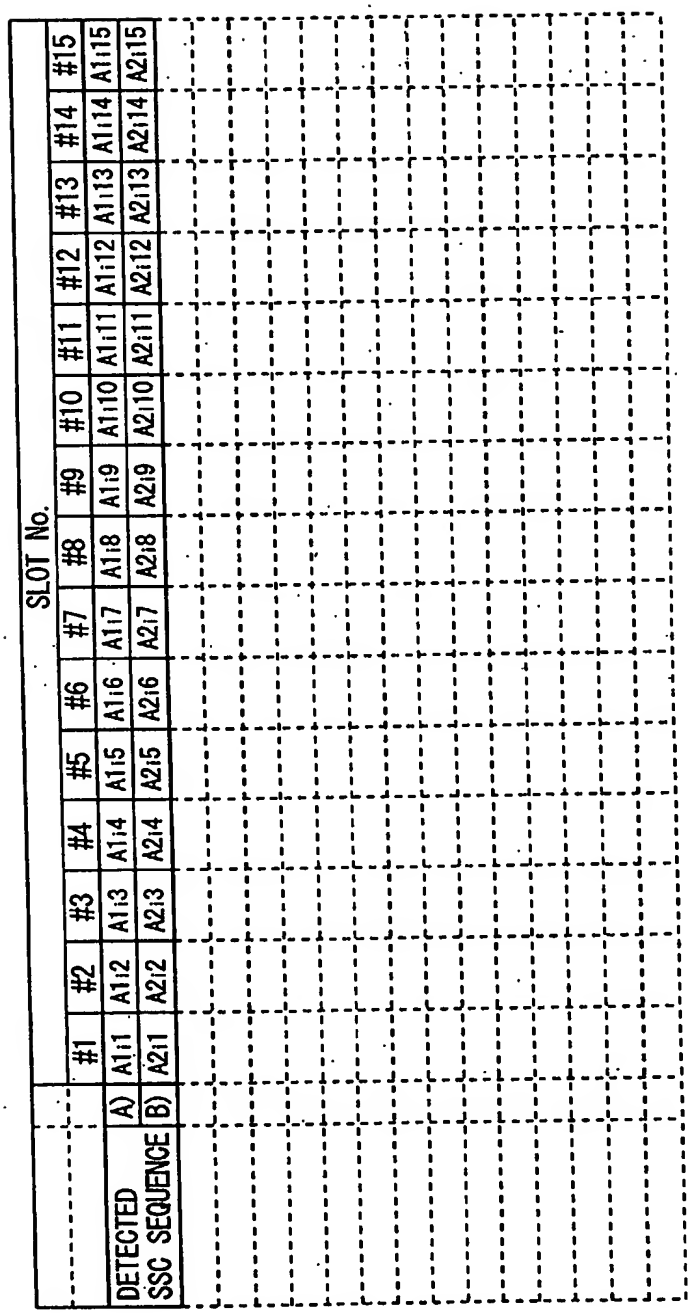
SLOT No.
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
#11
#12
#13
#14
#15
DETECTED SSC SEQUENCE
A)
B)
A1i1
A2i1
A1i2
A2i2
A1i3
A2i3
A1i4
A2i4
A1i5
A2i5
A1i6
A2i6
A1i7
A2i7
A1i8
A2i8
A1i9
A2i9
A1i10
A2i10
A1i11
A2i11
A1i12
A2i12
A1i13
A2i13
A1i14
A2i14
A1i15
A2i15

FIG. 12

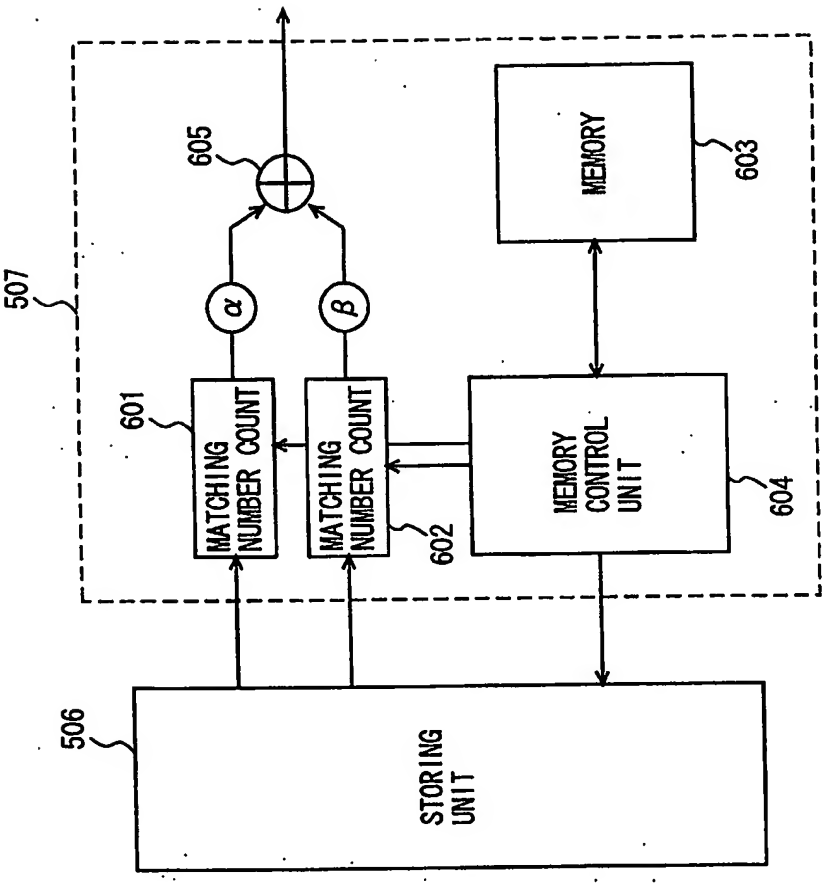
507
605
α
β
MEMORY
603
601
MATCHING NUMBER COUNT
MATCHING NUMBER COUNT
602
MEMORY CONTROL UNIT
604
506
STORING UNIT

FIG. 13

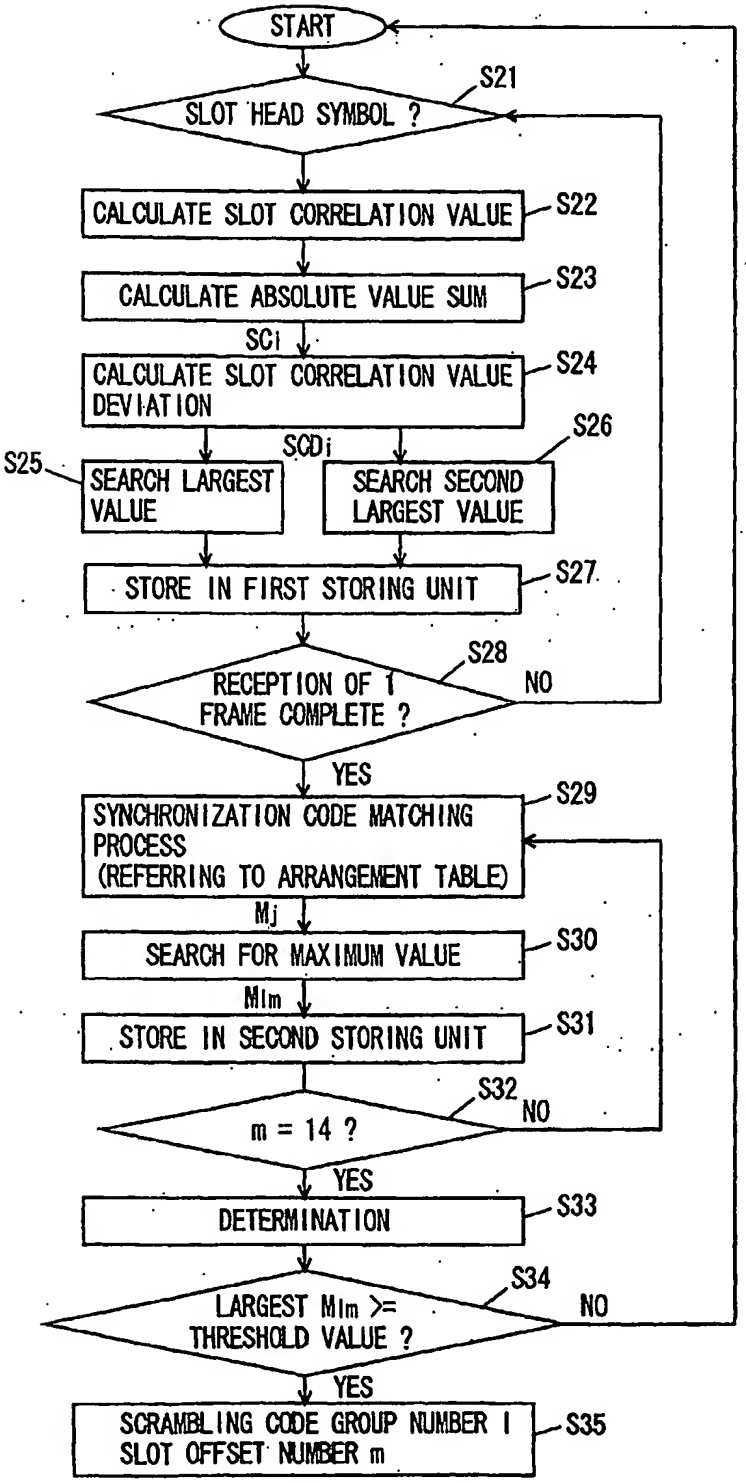
START
S21
SLOT HEAD SYMBOL ?
CALCULATE SLOT CORRELATION VALUE
S22
CALCULATE ABSOLUTE VALUE SUM
S23
SCi
CALCULATE SLOT CORRELATION VALUE DEVIATION
S24
SCDi
S26
S25
SEARCH LARGEST VALUE
SEARCH SECOND LARGEST VALUE
STORE IN FIRST STORING UNIT
S27
S28
RECEPTION OF 1 FRAME COMPLETE ?
NO
YES
S29
SYNCHRONIZATION CODE MATCHING PROCESS (REFERRING TO ARRANGEMENT TABLE)
Mj
SEARCH FOR MAXIMUM VALUE
S30
MIm
STORE IN SECOND STORING UNIT
S31
S32
m = 14 ?
NO
YES
DETERMINATION
S33
S34
LARGEST MIm >= THRESHOLD VALUE ?
NO
YES
SCRAMBLING CODE GROUP NUMBER I
SLOT OFFSET NUMBER m
S35

FIG. 14

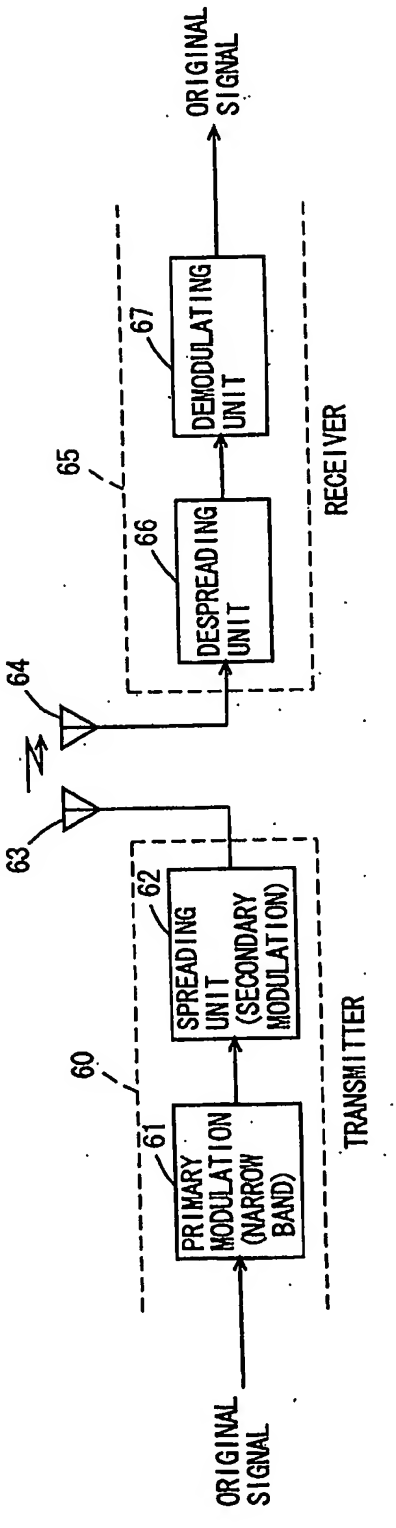
ORIGINAL SIGNAL
PRIMARY MODULATION (NARROW BAND)
61
SPREADING UNIT (SECONDARY MODULATION)
62
60
TRANSMITTER
63
64
DESPREADING UNIT
66
DEMODULATING UNIT
67
65
RECEIVER
ORIGINAL SIGNAL

FIG. 15

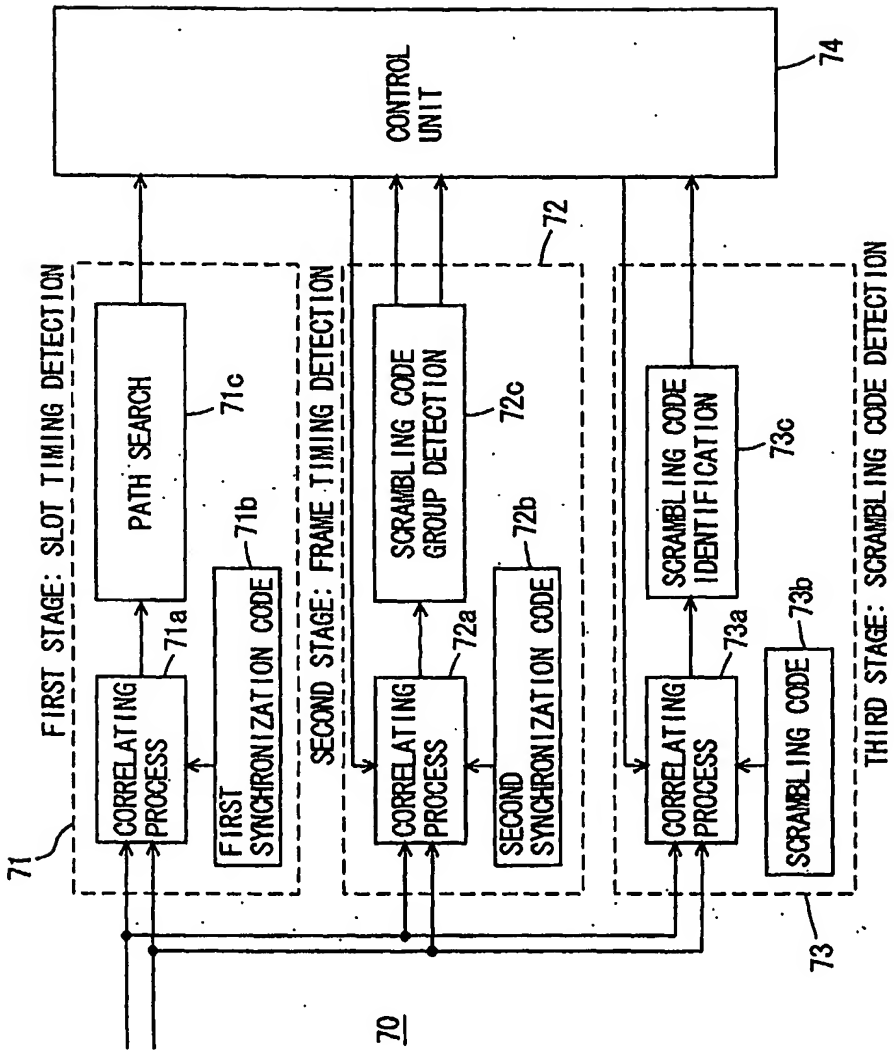
CONTROL UNIT
74
FIRST STAGE: SLOT TIMING DETECTION
SECOND STAGE: FRAME TIMING DETECTION
THIRD STAGE: SCRAMBLING CODE DETECTION
71
72
73
70
CORRELATING PROCESS
71a
PATH SEARCH
71c
FIRST SYNCHRONIZATION CODE
71b
CORRELATING PROCESS
72a
SCRAMBLING CODE GROUP DETECTION
72c
SECOND SYNCHRONIZATION CODE
72b
CORRELATING PROCESS
73a
SCRAMBLING CODE IDENTIFICATION
73c
SCRAMBLING CODE
73b

FIG. 16

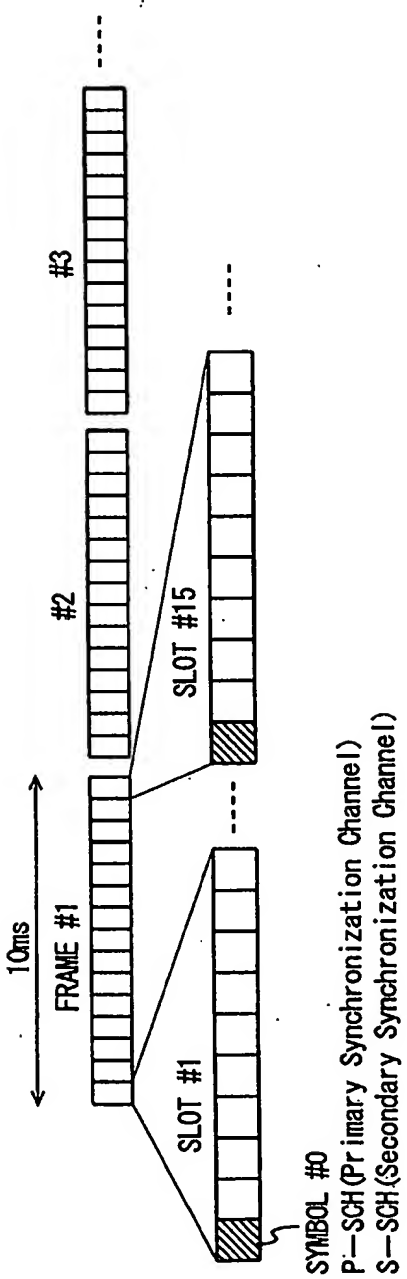
10ms
FRAME #1
#2
#3
SLOT #1
SLOT #15
SYMBOL #0
P-SCH(Primary Synchronization Channel)
S-SCH(Secondary Synchronization Channel)

FIG. 17

SCRAMBLING CODE GROUP No.	SLOT No.														
	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15
Group 1	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 2	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 3	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 4	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 5	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 6	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 7	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 8	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 9	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 10	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 11	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 12	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 13	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 14	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 15	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 16	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 17	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 18	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 19	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 20	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 21	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 22	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 23	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 24	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 25	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
⋮															
Group 48	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 49	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 50	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12
Group 51	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 52	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 53	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 54	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 55	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 56	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 57	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 58	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 59	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 60	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 61	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 62	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 63	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 64	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10